

Creating a digital I/O model for an inverter for PSpice

Source: Brian Hirasuna, Cadence Design Systems, March 2000

Overview

Here we show how create an inverter model for mixed-signal simulation with PSpice®.

Taking the measurements

Measurements or datasheet specifications should be obtained for the following:

- Propagation delay (l-h on the output of the inverter) from V_{il} on input waveform to V_{ih} on output waveform
- Propagation delay (h-l on the output of the inverter) from V_{ih} on input waveform to V_{il} on output waveform
- Switching times from 0% to 100%
- Input resistance
- Input capacitance
- Output capacitance
- Slope of low state V-I curve in switching region
- Slope of high state V-I curve in switching region
- Steady state resistances for low and high states
- V_{il} , V_{ih} , minimum and maximum input voltages

These measurements should be made with a fast ramp on the input.

Create the logic primitives and propagation delays

First use PSpice ‘U’ devices to model the logic and propagation delays.

Propagation delay is measured from V_{ih} (or V_{il}) on input waveform to V_{il} (or V_{ih}) on output waveform (since this is an inverter). Note that this differs from the way that most datasheets specify propagation delay = $V_{t,typ}$ on input waveform to $V_{t,typ}$ on output waveform. PSpice uses this “wider” definition of propagation delay to model the threshold region (from V_{il} to V_{ih}) as an “unknown” state.

The power supply nets, DVCC and DGND, are defined by power symbols (or globals) on the schematic.

```
.subckt invm A Y
+   optional: DPWR=DVCC DGND=DGND
+   params: MNTYMXDLY=0 IO_LEVEL=1
U1 inv DPWR DGND
+   A   Y
+   D_inv IO_inv MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
.ends
*
.model D_inv ugate (
+   tplhty=62ps ; propagation delay Vih,in to Vil,out (inverter)
+   tphlty=33ps ; propagation delay Vil,in to Vih,out
+   )
```

Create the UIO model

Next create the UIO model, which points to the specific AtoD and DtoA model which will get used. In addition steady state resistances, and 0% to 50% switching times are entered here.

```
.model IO_inv uio (
```

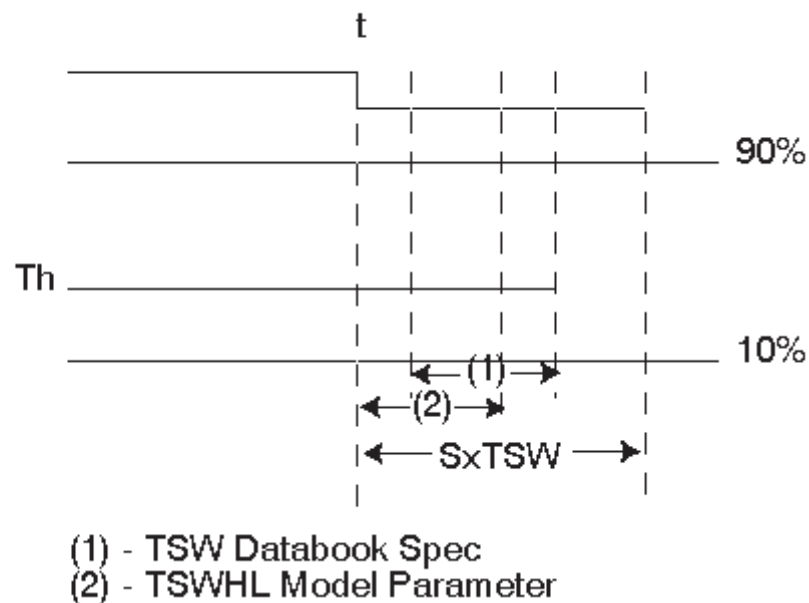
drvh and drvl are steady state resistances for high and low states

```
+   drvh=3.99k   drvl=1.03k
```

inld and outld are the input and output capacitance

```
+   inld=7.44fF   outld=6.77fF
```

The switching times TSWHL1 and TSWLH1 are subtracted from a devices propagation delay for devices which have a DtoA subcircuit created at their output. This compensates for the overlap in time between the propagation delay and the SxTSW switching times (in the input model below).



To find values for TSWHL1 and TSWLH1, run a transient analysis with capacitances in the model. Use a fast input ramp to examine a digital output (with no analog connections), and an analog output (connect the output of the inverter to a large resistor).

First fine tune t_{phl}. Start with t_{swlh1}=0. Measure the time from the digital transition (use a fast input ramp) to the V_{il} point (0.8v here) on the output analog waveform. This is 17ps. Set t_{swlh1}=17ps.

Now fine tune t_{plh}. Set t_{swlh1}=0. Measure the time from the digital transition to the V_{ih} point (2.0v here) on the output analog waveform. This is 19.5ps. Set t_{swlh1}=19.5ps.

```
+ AtoD1="AtoD_inv" DtoA1="DtoA_inv"
+ tswlh1= 17p ; picked so that digital transition is at Vil=0.8v
+ tswlh1 = 19.5p ; picked so that digital transition is at Vih=2v
```

DIGPOWER specifies the name of a power supply subckt to be used when an AtoD or DtoA interface is created. It is not necessary to include this line if the power supplies are defined on the schematic and the OPTIONAL parameters DPWR and DGND are defined for the logic and prop delay model (the invm subckt above).

```
*+ DIGPOWER="DIGIFPWR"
+)
```

Create the AtoD model

The AtoD model contains a digital output device, and the input resistance and capacitance. The digital output (or analog input) is on the input side of the gate.

```
.subckt AtoD_inv A D DPWR DGND
+params: CAPACITANCE=0
*
O1 A DGND DOinv DGTLNET=D IO_inv
C1 A DGND {CAPACITANCE+0.1fF} ; input capacitance
R1 A DGND 4.68MEG ; input resistance
.ends
```

Create the DtoA model

The DtoA model contains a digital input device and the output capacitance. The digital input (or analog output) is on the output side of the gate.

```
.subckt DtoA_inv D A DPWR DGND
+ params: DRVL=0 DRVH=0 CAPACITANCE=0
*
N1 A DGND DPWR DINinv DGTLNET=D IO_inv
C1 A DGND {CAPACITANCE+0.1fF} ; output capacitance
.ends
```

Create the digital input (analog output) model

In the digital input model we specify the switching times from 0% to 100%, and the dynamic resistance to the hi and lo node for each state. s0rlo is the slope of the low V-I curve in switching region. s1rhi is the slope of the high V-I curve in switching region. Other values are of secondary importance, but should be sufficiently large.

```
.model DINinv dinput (
+   s0name="0"  s0tsw=20ps  s0rlo=10    s0rhi=10k
+   s1name="1"  s1tsw=20ps  s1rlo=50MEG s1rhi=1k
+   s2name="X"  s2tsw=20ps  s2rlo=10k   s2rhi=10k
+   s3name="R"  s3tsw=20ps  s3rlo=10k   s3rhi=10k
+   s4name="F"  s4tsw=20ps  s4rlo=10k   s4rhi=10k
+   s5name="Z"  s5tsw=20ps  s5rlo=1G    s5rhi=1G
+)
```

Create the digital output (analog input) model

The digital output is a state transition table which is cyclically traversed to find the next state (so the order is important).

```
.model DOinv doutput (
*** Unknown state between Vil and Vih
+   s0name="X"  s0vlo=0.8  s0vhi=2.0
*** 0 state between minimum input voltage and Vil
+   s1name="0"  s1vlo=-1.5 s1vhi=0.8
*** Two Rising states from Vil to Vih, with a small overlap
*** at the threshold voltage
+   s2name="R"  s2vlo=0.8  s2vhi=1.4
+   s3name="R"  s3vlo=1.3  s3vhi=2.0
*** A second unknown state between Vil and Vih
+   s4name="X"  s4vlo=0.8  s4vhi=2.0
*** 1 state between Vih and maximum input voltage
+   s5name="1"  s5vlo=2.0  s5vhi=6
*** Two Falling states from Vih to Vil, with a small overlap
*** at the threshold voltage
+   s6name="F"  s6vlo=1.3  s6vhi=2.0
+   s7name="F"  s7vlo=0.8  s7vhi=1.4
+)
```

The complete model of the inverter:

```
.subckt invm A Y
+   optional: DPWR=DVCC DGND=DGND
+   params: MNTYMXDLY=0 IO_LEVEL=1
U1 inv DPWR DGND
+   A Y
+   D_inv IO_inv MNTYMXDLY={MNTYMXDLY} IO_LEVEL={IO_LEVEL}
.ends
*

.model D_inv ugate (
```

```

+     tplhty=62ps      ; propagation delay Vih,in to Vil,out (inverter)
+     tphlty=33ps     ; propagation delay Vil,in to Vih,out
+     )

.model IO_inv uio (
+     drvvh=3.99k  drvl=1.03k
+     AtoD1="AtoD_inv"  DtoA1="DtoA_inv"
+     tswhl1= 17p    ; picked so that digital transition is at Vil=0.8v
+     tswlh1 = 19.5p ; picked so that digital transition is at Vih=2v
*+     DIGPOWER="DIGIFPWR"
+)

.subckt AtoD_inv  A D  DPWR DGND
+params: CAPACITANCE=0
*
O1  A DGND DOinv DGTLNET=D IO_inv
C1  A DGND {CAPACITANCE+0.1fF} ; input capacitance
R1  A DGND 4.68MEG ; input resistance
.ends

.subckt DtoA_inv  D A  DPWR DGND
+params: DRVL=0 DRVH=0 CAPACITANCE=0
*
N1  A DGND DPWR DINinv DGTLNET=D IO_inv
C1  A DGND {CAPACITANCE+0.1fF} ; output capacitance
.ends

.model DINinv dinput (
+     s0name="0"  s0tsw=20ps  s0rlo=10      s0rhi=10k
+     s1name="1"  s1tsw=20ps  s1rlo=50MEG   s1rhi=1k
+     s2name="X"  s2tsw=20ps  s2rlo=10k     s2rhi=10k
+     s3name="R"  s3tsw=20ps  s3rlo=10k     s3rhi=10k
+     s4name="F"  s4tsw=20ps  s4rlo=10k     s4rhi=10k
+     s5name="Z"  s5tsw=20ps  s5rlo=1G      s5rhi=1G
+)

.model DOinv doutput (
+     s0name="X"  s0vlo=0.8  s0vhi=2.0
+     s1name="0"  s1vlo=-1.5 s1vhi=0.8
+     s2name="R"  s2vlo=0.8  s2vhi=1.4
+     s3name="R"  s3vlo=1.3  s3vhi=2.0
+     s4name="X"  s4vlo=0.8  s4vhi=2.0
+     s5name="1"  s5vlo=2.0  s5vhi=6
+     s6name="F"  s6vlo=1.3  s6vhi=2.0
+     s7name="F"  s7vlo=0.8  s7vhi=1.4
+)
*$

```

© 2000 Cadence Design Systems, Inc. All rights reserved. Cadence, the Cadence logo, and PSpice are registered trademarks of Cadence Design Systems, Inc. All others are properties of their respective holders.