

CADENCE AND CRAY INC.

Cray Meets Aggressive ASIC Design Schedule, Leveraging Results from Encounter Test to Accelerate System Bring-Up

CORPORATE PROFILE

- Cray Inc. is the global leader in high-performance computing (HPC), producing supercomputing systems to meet the toughest computational challenges

DESIGN CHALLENGE

- Create a 4-million gate ASIC on a nine-month design schedule to meet critical market window
- Integrate legacy components into new design
- Find a vendor to address the physical design and complete DFT

CADENCE SOLUTION

- Partnered with Cray to complete the physical design and address the DFT challenge

CADENCE PRODUCTS AND SERVICES

- Cadence Encounter® digital IC design platform, including Encounter Test, Encounter RTL Compiler, and SoC Encounter™
- NC-Verilog®, part of the Cadence Incisive® functional verification platform
- Cadence VCAD Engineering Services

“Partnering with the Cadence VCAD engineering team enabled us to successfully tapeout our complex ASIC design and meet an aggressive time-to-market goal. Cadence completed our physical design and addressed our design-for-test (DFT) challenge, delivering high-quality test vectors that worked the first time, eliminating the need for debug and accelerating our system bring-up by days.”

Dennis Vollrath, Threadstorm Project Manager, Cray Inc.

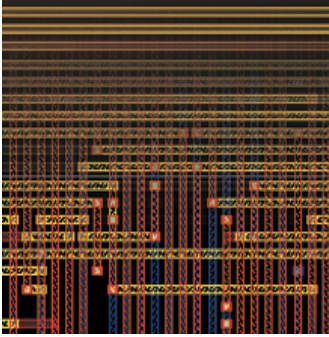
Putting the “Super” in Computing Since 1972

Headquartered in Seattle, Washington, Cray Inc. continues the high-performance computer innovation that was started by Seymour Cray more than three decades ago. The name Cray has become synonymous with supercomputing. The company has evolved with the needs of academia, government, and industry to maintain global leadership in supercomputing.

Cray was embarking on a new complex ASIC design, code-named Threadstorm. In order to achieve their aggressive nine-month design schedule, the team needed to outsource large portions of the project. “We have a strong, long-term relationship with Cadence, and have partnered with the Cadence VCAD team on multiple on-site support projects in the past,” said Dennis Vollrath, Threadstorm project manager at Cray. “For the Threadstorm project, we were looking for a more turnkey level of support than we have needed in the past. Cadence was there with the tools and expertise to address all of our project requirements.”

Cadence and Cray Collaborate to Meet Time-to-Market Needs

The Threadstorm team outsourced two areas of their design to the Cadence VCAD team. “We asked Cadence to handle the physical design and design for test (DFT),” continued Vollrath. Threadstorm is a 0.13 μ TSMC processor design. “Our plan was to leverage an existing system design for Threadstorm to speed our process,” said Vollrath. “This created some design challenges, particularly in the area of DFT.”



“The Cray and Cadence teams were able to work together to achieve a common goal with excellent quality of results. We look forward to our next project, knowing that the strength of our resources stretches across two teams rather than one.”

Dennis Vollrath, Threadstorm Project Manager, Cray Inc.

Cadence Encounter Platform Addresses DFT Challenge from RTL to Silicon

One of the primary challenges that the Cadence VCAD team faced on the Threadstorm project was the need to incorporate pre-existing scan chains into the new design. Only certain areas of certain blocks in the legacy design had been scanned.

The VCAD team ran DFT synthesis with Encounter RTL Compiler global synthesis to understand the segments of the legacy scan chain, and to integrate those segments with the new design sections in preparation for a hand-off to Encounter Test ATPG. This ensured that the team would be able to maximize test coverage in the design.

The Threadstorm design was divided into seven blocks, or macros, and each would be floorplanned individually and assembled in the final chip. To address this, the VCAD team used Encounter RTL Compiler to implement a new methodology, creating abstract scan models for each block so that they could be hooked up at the assembly stage of the design process.

Cadence Encounter Test Delivers High-Quality Test Vectors, Eliminating Need for Debug

Using Encounter Test for ATPG enabled the VCAD team to achieve very high test coverage. As part of the DFT flow, they used Encounter RTL Compiler to quickly identify problem areas in the design with regard to testability, further increasing test coverage results.

In addition, the team delivered high-quality test vectors, verified by the Cadence Incisive NC-Verilog simulator, that worked the first time on the tester. Since they were able to avoid silicon debug, the VCAD team was able to deliver tested parts to Cray within 24 hours.

“Partnering with the Cadence VCAD engineering team enabled us to successfully tape out our complex ASIC design and meet an aggressive time-to-market goal,” said Vollrath. “Cadence completed our physical design and addressed our DFT challenge, delivering high-quality test vectors that worked the first time, eliminating the need for debug and accelerating our system bring-up by days.”

Long-Term Partnership Between Cray and Cadence Pays Dividends

“Sharing responsibility for such major elements of the design on such a tight schedule requires trust and collaboration,” said Vollrath. “The Cray and Cadence teams were able to work together to achieve a common goal with excellent quality of results. We look forward to our next project, knowing that the strength of our resources stretches across two teams rather than one.”



FOR MORE INFORMATION, EMAIL INFO@CADENCE.COM OR LOG ON TO WWW.CADENCE.COM

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