



how big can you dream?™

CADENCE AND INTELLITECH

NC-VHDL, NC-VERILOG, AND NC-SIM FOR FPGA SIMULATION WITH SYNPLIFY AND XILINX

“NC-VHDL, NC-Verilog, and NC-Sim are best-in-class tools that we highly recommend to others in our industry. Our partnership with Cadence has been a win-win for us and our customers.”

Mike Ricchetti
Chief Technology Officer, Intellitech

CORPORATE PROFILE

- Technology leader in scan-based debug and test solutions. The products allow engineers to debug ICs and systems without probes.

DESIGN CHALLENGE

- Lower customers' product cost by providing a standardized on-board architecture for FPGA logic configuration and embedded test
- Verify quality of TEST-IP implementations
- Adopt simulation tools that spur productivity and fit well into a seamless FPGA design flow

CADENCE SOLUTION

- Well-integrated overall design and simulation flow targeting Xilinx FPGAs
- Highly productive debugging environment

CADENCE PRODUCTS AND SERVICES

- NC-VHDL, NC-Verilog®, NC-Sim
- Cadence Capture and Layout Plus

POWERFUL FPGA DESIGN AND SIMULATION FLOW FOR INNOVATIVE DFT TECHNOLOGY

The TEST-IP product family from Intellitech provides customers with an architecture to make their products self-testable and logic upgradeable in the field.

Since the TEST-IP design flow can be used with Xilinx FPGAs, Intellitech needed a powerful, easy-to-use, and well-integrated FPGA design and simulation flow. The combination of Cadence® NC-VHDL, NC-Verilog®, and NC-Sim simulation environments and Synplify FPGA synthesis fulfilled all of the needs of Intellitech. Intellitech found that debugging with NC-VHDL, NC-Verilog, and NC-Sim could be performed much quicker than with other tools available, and that the Cadence tools were easy-to-learn, easy-to-use, and highly cost-effective. The debugging environment provided by the Cadence products proved extremely valuable, helping the company meet its customers' delivery goals and expectations for product quality.

DFT TECHNOLOGY LEADER INNOVATES WITH TEST-IP

Intellitech Corporation is a leading provider of tools for scan-based electronic design verification, silicon debug, and test. The Intellitech expertise in Design-for-Test (DFT) is manifested in its SoC, IC, PCB, and system solutions—enabling customers to debug prototype designs and test production quantities without physical probing. These debug, test, and analysis tools allow customers to bring high quality products to market faster by reducing prototype hardware verification times. Customers realize cost and time savings by the re-use of tests through all phases of a product's life. The new TEST-IP family further reduces customers' costs by embedding the manufacturing tests and FPGA programming in the product itself. The Durham, New Hampshire-based company was formed in 1988 and has a long history of success using Cadence board-level products.

Intellitech has developed a family of products called TEST-IP™ to complement their external 1149.1 based test and programming equipment. This patent-pending technology is targeted for major original equipment manufacturers (OEMs) that create electronic systems that need automatic structural POST (Power on Self-Test), multi-device FPGA configuration and in-the-field logic upgrade capability.

The TEST-IP family consists of a set of ICs or IP that can be implemented in customer products to make them self-testable and in-the-field logic upgradeable. It centralizes in-system FPGA programming resources, so system logic can be easily upgradeable in-the-field or even remotely over the Internet. Since the TEST-IP architectures do not require a CPU or software to operate, the solution has a low cost of parts and does not use any system resources. One member of the family, SystemBIST™, not only configures all FPGAs and CPLDs but reduces customers' manufacturing test cost as it enables digital structural PCB test to be embedded in the customer's product. When digital based tests can be performed automatically in-system, then traditional in-circuit testing will be reduced to just simple, low cost analog tests reducing test time and ICT fixture costs.

The TEST-IP family lowers FPGA parts costs, lowers manufacturing test costs, improves product quality and field service. It improves time-to-market, and cuts engineering time, satisfying DFT requirements by providing a pre-designed solution and architecture for customers to include in their system.

An important market for TEST-IP is the base of customers who need to be able to upgrade, configure, or test products that use FPGAs. Intellitech, therefore, needed to establish a strong flow for designing and simulating FPGA devices, such as Xilinx FPGAs, and verifying their quality. TEST-IP implementations are used in a variety of configurations and target devices so it was important that this environment be easy-to-use and highly productive.

NC-VHDL, NC-VERILOG, AND NC-SIM PROVIDE POWERFUL, COST-EFFECTIVE, WELL-INTEGRATED ENVIRONMENT

Intellitech selected Synplify from Synplicity as its FPGA synthesis tool, and needed to complement it with a strong suite of simulation products to complete the FPGA design flow. "Our experience with Cadence PCB products was good, so it was a natural evolution for us to look to Cadence for our FPGA simulation needs," said CJ Clark, President and CEO of

Intellitech. "We examined NC-VHDL, NC-Verilog, and NC-Sim, and found that they offer the debugging environment we needed along with excellent price-performance. Our customers count on our TEST-IP products to be flawless, and so the accuracy of simulation performed by these Cadence products is essential."

"Since NC-VHDL, NC-Verilog, and NC-Sim are desktop tools, they are very cost-effective," added Mike Ricchetti, Chief Technology Officer for Intellitech. "We found them to be easy to learn and our designers quickly became productive with them."

ALL GOALS SATISFIED IN FULL

Installation of NC-VHDL, NC-Verilog, and NC-Sim was quick, and Intellitech designers soon commenced using this flow in production to debug designs for early adopter customers of TEST-IP.

"We were successful in meeting our target dates for our customers, and the Cadence tools contributed substantially to this success," reported Ricchetti. "Because the tools are easy to use and well integrated, we could very quickly find and repair all the problems in our early designs. NC-VHDL, NC-Verilog, and NC-Sim met all our expectations and helped us satisfy all our customers' goals."

The early adopters of TEST-IP found this Intellitech technology to be easy to incorporate into their PCB products. These customers have benefited from reduced design time and cost of testing. Their products have improved test coverage because they include Intellitech innovations and patent pending technology.

"For debugging in a simulation environment, the Cadence tools are much faster than anything else available in the industry," said Clark. "Now we use them on a daily basis in our work, enhancing several TEST-IP implementations and improving their value to our customers."

"NC-VHDL, NC-Verilog, and NC-Sim are best-in-class tools that we highly recommend to others in our industry," concluded Ricchetti. "Our partnership with Cadence has been a win-win for us and our customers."

More information on Intellitech may be found at: www.intellitech.com.



FOR MORE INFORMATION

Email info@cadence.com or log on to www.cadence.com

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