

ASSURA LAYOUT VS. SCHEMATIC VERIFIER

Cadence® Assura® Layout vs. Schematic (LVS) Verifier is part of the design verification suite of tools within the Virtuoso® custom design platform. Assura LVS ensures that the layout connectivity of the physical design matches the logical design represented by the schematic or netlist before tapeout. By automatically extracting devices and nets formed across layout hierarchy and comparing them to the schematic netlist, Assura LVS provides fast, efficient verification in both interactive and batch mode.

THE VIRTUOSO CUSTOM DESIGN PLATFORM

When design objectives dictate manipulating precise analog quantities—voltages, currents, charges, and continuous ratios of parameter values such as resistance and capacitance—companies turn to custom design. Full-custom design maximizes performance while minimizing area and power. However, it requires significant handcrafting by a select set of engineers with very high skill levels. In addition, custom analog circuits are more sensitive to physical effects, which are exacerbated at new, nanometer process nodes.

The Virtuoso custom design platform accelerates the design of custom ICs across various process nodes. By selectively automating aspects of custom analog design and providing advanced technologies integrated on a common database, it allows engineers to focus on precision crafting their designs—without sacrificing creativity to repetitive manual tasks.

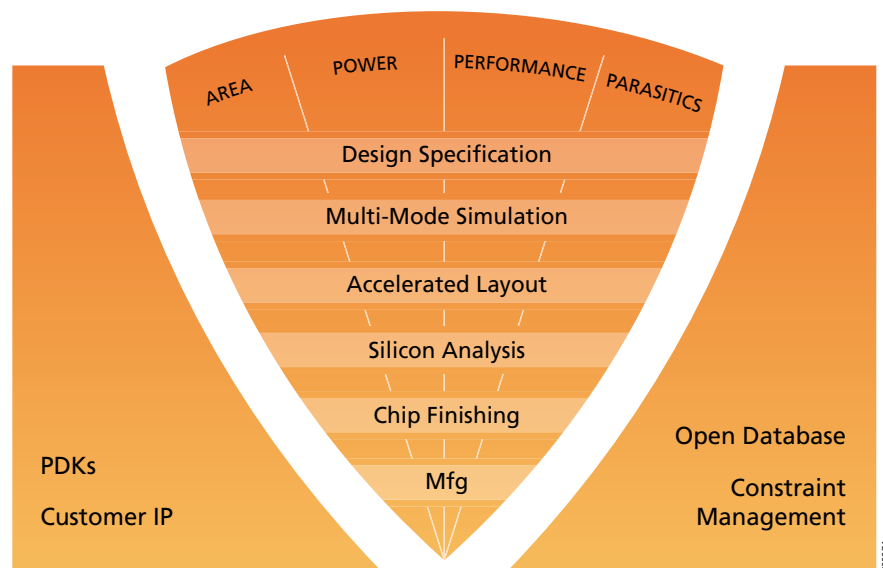


Figure 1: All components of the Virtuoso platform work together to support fast, silicon-accurate differentiated custom silicon

ASSURA LVS

As part of the Virtuoso custom design platform, Assura LVS enables design teams to check, identify, and correct layout connectivity and physical and logical mismatch errors to achieve design sign-off before tapeout. With a GUI-guided debugging environment and hierarchical processing techniques, Assura LVS reduces the overall verification cycle time, especially for designs with high complexity and many levels of layout hierarchy. Assura LVS, along with Assura DRC and Assura RCX, provides the best choice for doing fast and accurate silicon analysis of your custom designs.

BENEFITS

- Simplifies design process with a common database for data transfer within the Virtuoso custom design platform
- Accelerates design-to-volume with production-proven interactive LVS debugger
- Reduces re-spins by eliminating connectivity and mismatch errors before tape-out
- Ensures success in analog mixed-signal design with support of mixed netlist and special devices

FEATURES

GUI-GUIDED LVS DEBUG ENVIRONMENT

Assura LVS offers a GUI debug environment that guides you through the debugging process and helps resolve LVS errors. Once the LVS run is complete, you can choose to open the LVS debug tools, such as the short locator and rewire functions, from the pop-up window to examine and correct the errors (see Figure 2).

The guided-debugging process starts when the "Yes" button is pushed. Figure 3 shows the extraction errors, such as shorts, that need to be fixed. With the GUI-guided LVS debugger, you can easily locate the shorts and correct the error.

The rewire function (see Figure 4) is similar to that of Diva® verification. It helps you understand which changes are necessary to

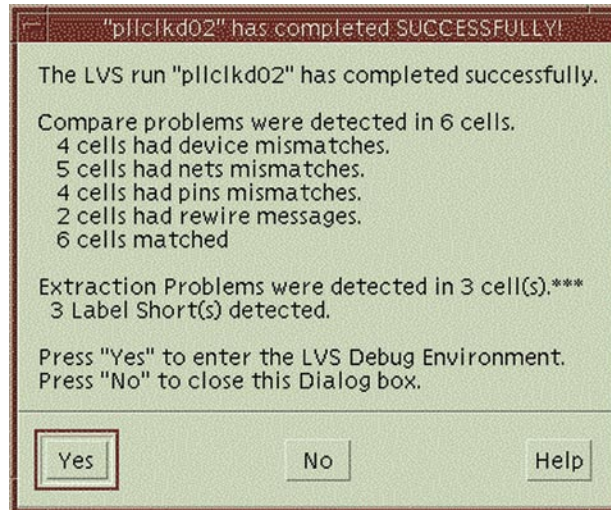


Figure 2: GUI-guided LVS debug environment shows the compare and extraction errors after the LVS run is complete



Figure 3: GUI-guided LVS debug environment helps locate and fix the layout easily

shorts in

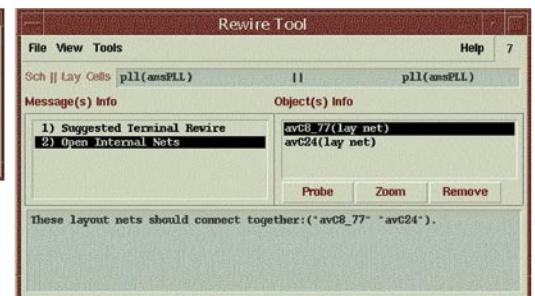


Figure 4: The rewire function in the GUI-guided LVS debug environment advise how to fix rewire errors

correct mistakes and tells you exactly how to fix the design. This unique approach will significantly reduce your total LVS debugging and overall verification runtime.

SUPPORT OF MIXED-SIGNAL DESIGNS

Assura LVS has the ability to recognize standard and special devices (n-terminal devices, drawn inductors, multi-emitter/collector bipolar transistors, STI, ROMs, etc.), making it an excellent choice for mixed-signal designs. All devices extracted

by Assura LVS are automatically netlisted and passed onto Assura RCX to avoid "double-counting" during parasitic extraction. Assura LVS also has the capability to address mixed-signal designs that need to combine schematics from CDL, SPICE, and Verilog® languages.

INTERACTIVE AND BATCH VERIFICATION

Assura LVS can perform layout vs. schematic verification in both interactive and batch mode. The ability to perform

physical verification interactively within the Virtuoso custom design platform is especially important for design teams to hand-craft their full custom ICs in order to maximize silicon performance and yield. The Assura LVS interactive use model including schematic to layout cross-probing is very similar to that of Diva verification. Batch verification is available for designers who prefer to script their verification process. Only a single LVS file is needed for both interactive and batch verification.

HIERARCHICAL PROCESSING

Assura LVS uses hierarchical processing techniques to perform layout vs. schematic verification, resulting in higher performance and capacity. Designs that utilize various levels of layout hierarchy, such as memory, can be efficiently checked with the hierarchical processing techniques. LVS errors reported hierarchically help users locate them quickly and solve the problem at the root cause as errors in the same hierarchy only have to be corrected once.

UNIFIED ENVIRONMENT

Assura LVS is an integral part of the Virtuoso custom design platform and every release of Assura LVS is flow tested within the platform methodology. The unified environment makes it easy for users to design custom ICs starting from physical layout design to physical verification to parasitic extractions to simulation and analysis before tapeout, leading to increased design productivity, chip performance, and silicon yield.

MASTER KEY

The master key is a feature of the Cadence customer-focused adoption program with Assura physical verification, aiding customers during the transition of Diva or Dracula® products to Assura verification. The master key enables you to convert existing Diva or Dracula licenses to Assura licenses such that Assura licenses can be used to run Diva and Dracula tools during the transition. Please check with your Cadence sales representative for more detail of the master key.

SPECIFICATIONS

DEVICE EXTRACTION AND NETLIST SUPPORT

- Drawn (spiral & center-tap) inductor parameters
- CMOS, bipolar, diodes, n-terminal devices, ROMs, etc.
- STI effects (SA/SB parameters)
- Expanded CDL syntax and mixed netlist (schematic, CDL, Verilog)

COMPREHENSIVE GUI-GUIDED LVS DEBUGGING TOOLS

- Extraction errors
 - Short locator
 - Open locator
 - Malformed device tool
- Comparison errors
 - Nets mismatch
 - Devices mismatch tool
 - Pins mismatch tool
 - Parameters mismatch tool
 - Rewire tool
- Hypertext netlist form displays the schematic netlist that corresponds to your layout and allows hierarchical cross-probing for blocks, cells, devices, nets, and pins directly from the displayed schematic netlist
- Net and device probing for locating matched and unmatched nets and connected devices in the layout or schematic window
- Command interpreter window (CIW) logs user's actions for future use

PERFORMANCE AND CAPACITY

- Patented hierarchical algorithms (cell repetition analysis, auto-adaptive partitioning, and auto-array recognition) process large volumes of data
- Multiprocessor support for reduction in runtime (uses both rules-based and data-based parallelism to optimize runtimes automatically)
- Restart function for interrupted jobs saves precious CPU time
- Support 32-bit on all platforms and 64-bit on selected platforms

EASY-TO-USE GUI

- Tightly integrated with Virtuoso Layout Editor and Virtuoso Analog Design Environment
- Hierarchical error reporting and cross-probing
- Access layout data in edit or read-only modes within Virtuoso Layout Editor
- Fast error correction using edit-in-place or descend modes within Virtuoso Layout Editor
- Show errors by rule type or by layout cell
- Hierarchical cross-probing for blocks, cells, devices, nets, and pins
- Immediate error and warning messages during interactive sessions via command interpreter window (CIW)
- Remote job submission/LSF support
- User-configurable commands allow flexible comparison of non-standard parameters
- Easy, programmable rule syntax extends Assura's capabilities during rule file creation, device extraction and netlist comparison operations

DESIGN INPUTS

- Cadence CDBA database (DFII) (layout and schematics)
- OpenAccess database
- GDSII layout data (single or multiple GDSII files)
- SPICE/CDL netlists
- Verilog netlists
- Diva, Vampire, or Assura rules

DESIGN OUTPUTS

- Cadence CDBA database (DFII) (layout and schematics)
- OpenAccess database
- GDSII layout data (single or multiple GDSII files)
- SPICE/CDL netlists
- Graphical error markers and textual reports for debugging purposes

PLATFORM/OS

- Sun/Solaris
- HP-UX
- IBM AIX
- Linux (Red Hat)

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
 - Collaborative approach and design infrastructure—virtual teaming
 - Proven methodology and flow tuned to your design environment
 - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
 - Over 80 instructor-led courses—certified instructors, real-world experience
 - More than 25 Internet Learning Series (ILS) online courses
- Cadence customer support that keeps your design team productive
 - Cadence applications engineers provide technical assistance
 - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, 7 days a week

CADENCE PDK AND FOUNDRY SUPPORT

Assura LVS rule files are fully qualified for use with the Cadence process design kits (PDKs), which can be obtained for free from the merchant foundries. These kits are developed and tested by Cadence and supplied to the foundries to support your success in designing chips with particular foundry processes. Please check your merchant foundry web site for the availability of PDK and Assura LVS rule files.

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