

DIVA PHYSICAL VERIFICATION

Diva® physical verification is part of the design verification suite of tools within the Virtuoso® custom design platform. It provides real-time physical verification of cells, blocks, and small IC designs. With strong interactivity for identifying and correcting layout errors, Diva verification is ideal for hand-crafting custom designs.

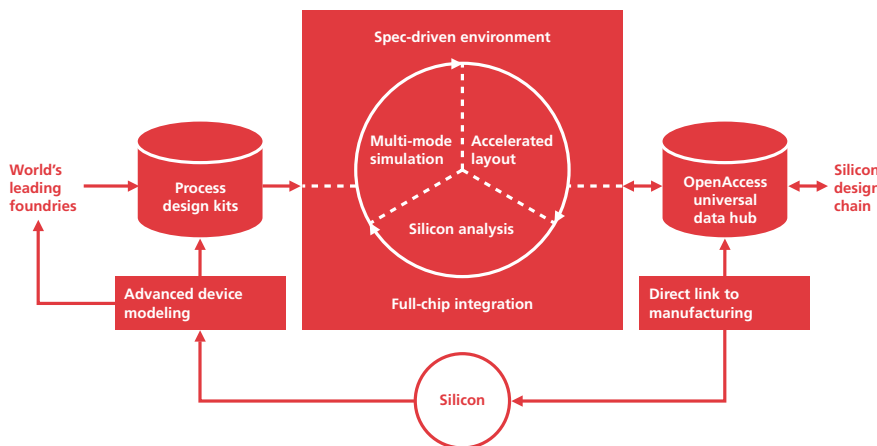


Figure 1: Virtuoso custom design platform

VIRTUOSO CUSTOM DESIGN PLATFORM

The Virtuoso custom design platform is a comprehensive system for fast, silicon-accurate design and is optimized to support “meet-in-the-middle” design methodologies such as advanced custom design. Virtuoso includes the industry’s only specification-driven environment, multi-mode simulation with common models and equations, vastly accelerated layout, advanced silicon analysis for 0.13 microns and below, and a full-chip, mixed-signal integration environment. The Virtuoso platform is available on the Cadence® CDBA database and the industry-standard OpenAccess database. With the Virtuoso platform, design teams can quickly design silicon that is right and on time at process geometries from one micron to 90 nanometers and beyond.

DIVA VERIFICATION PRODUCTS

As part of the Virtuoso custom design platform, Diva tools enable design teams to interactively identify and correct design rule errors and layout and schematic mismatches. Also, Diva verification extracts layout parasitics and allows post-layout simulations with parasitics to be performed without leaving the Virtuoso custom design platform. Operating directly on the layout database, it eliminates the need for time-consuming data translation. With thousands of tapeouts, Diva verification is one of the most widely used physical verification tool suites for checking and optimizing cells, blocks, and small IC designs.

BENEFITS

- Simplifies the design process with a common database for data transfer within the Virtuoso custom design platform
- Provides a robust interactive physical verification flow for custom designs
- Accelerates design-to-volume with a production-proven interactive physical verification tool suite
- Reduces re-spins by eliminating design layout errors before tape-out

FEATURES

INTERACTIVE VERIFICATION

Diva verification products are fully integrated within the Virtuoso custom design platform to provide design teams with an interactive environment to hand-craft and optimize custom designs in order to achieve the precision required for designing analog, RF, library, and analog mixed-signal chips (see *Figure 2*). Interactive checking reduces the layout verification process because it provides immediate feedback and prevents errors from accumulating. With a simple menu selection, you can check the entire design, the design within a user-defined window, or only those portions of the design that have been changed since the last verification run.

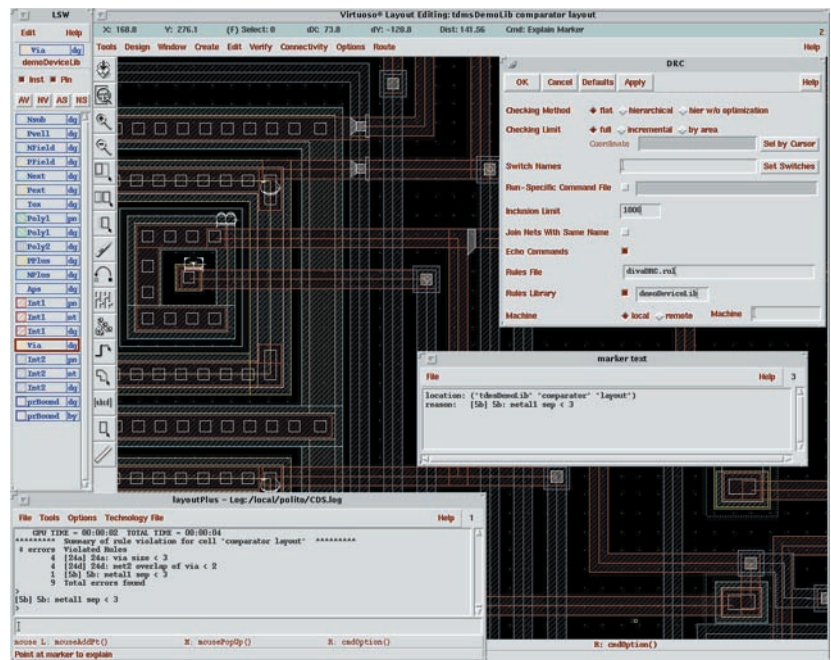


Figure 2: Interactive verification using Diva DRC within the Virtuoso Layout Editor

DIVA DESIGN RULE CHECKER (DRC)

Diva DRC provides numerous commands and modifiers to develop DRC checks for verifying your fabrication design rules. It includes user-defined options that allow you to run commands on specific criteria, such as parallel and opposite edges only, electrically-connected or unconnected figures, or line lengths that meet specified criteria. The results of each operation can be used by subsequent checks or stored in the database for later reference. Diva DRC also provides incremental or window-checking features that can reduce runtime of larger designs by only rechecking altered areas.

DIVA LAYOUT VS. SCHEMATIC (LVS) VERIFIER

Diva LVS is capable of recognizing and extracting device parameters from all integrated circuit technologies. For CMOS technologies, Diva LVS has a predefined device description that greatly enhances the speed of device extraction. For other technologies, such as bipolar and silicon germanium (SiGe), a user-configured command file

simplifies the identification of any device. This makes the device extractor extremely versatile in that it can support a wide spectrum of design methodologies and process technologies (see *Figure 3* on next page).

Diva LVS also provides the ability to run electrical-connectivity checks on both logical and physical network representations. This tool contains advanced features such as checking for compliance with user-defined fanout rules and converting a transistor-level circuit to gate-level, including consolidation of series and parallel devices.

In most IC applications, the layouts and schematics are rarely identical. There are variations such as permuted, interchanged, and combined devices because of layout or schematic optimization. Diva LVS handles these variations, permitting accurate circuit comparisons without false errors. Consolidation options reduce groups of devices of the same type connected in series or parallel into a single device for comparison. In addition, a rewire option allows designers to rapidly locate and correct hook-up errors. When comparing a parameter, Diva

LVS permits complete control over which parameters to check and how the comparison will be made for each device type. For example, parameters may be required to match exactly or within a user-defined tolerance.

Diva LVS also offers a macro-level LVS option that provides users with a method for performing a black-box LVS. This feature allows users to verify blocks or macros once and only verify the connectivity to those blocks at a higher level during subsequent LVS runs. Users can achieve significant reductions in LVS runtimes by employing this use model.

DIVA PARASITIC EXTRACTOR (RCX)

Diva RCX allows design teams to provide the layers, coefficients, bend factors, and other necessary criteria in equations that will perform parasitic resistance and capacitance calculations. An extracted resistance network containing associated distributed capacitance is formed. During the network reduction phase, the values of capacitance are consolidated and associated with each final resistor. This RC pair or group may be represented in a "pi" or "T" formation. All parasitic devices are graphically displayed including the values measured for each resistor and capacitor. This RC network is combined with the circuit netlist to form a final netlist containing designed and parasitic devices. The final netlist can then be simulated with SPICE, Virtuoso Spectre® Circuit Simulator, or other similar simulators to determine the exact electrical performance of the layout. Diva RCX includes a three-body/two-dimensional (charge-sharing) capacitance extraction capability, providing higher extraction accuracy.

See Figure 4 for an example of parasitic probing of Diva RCX results backannotated on the schematic.

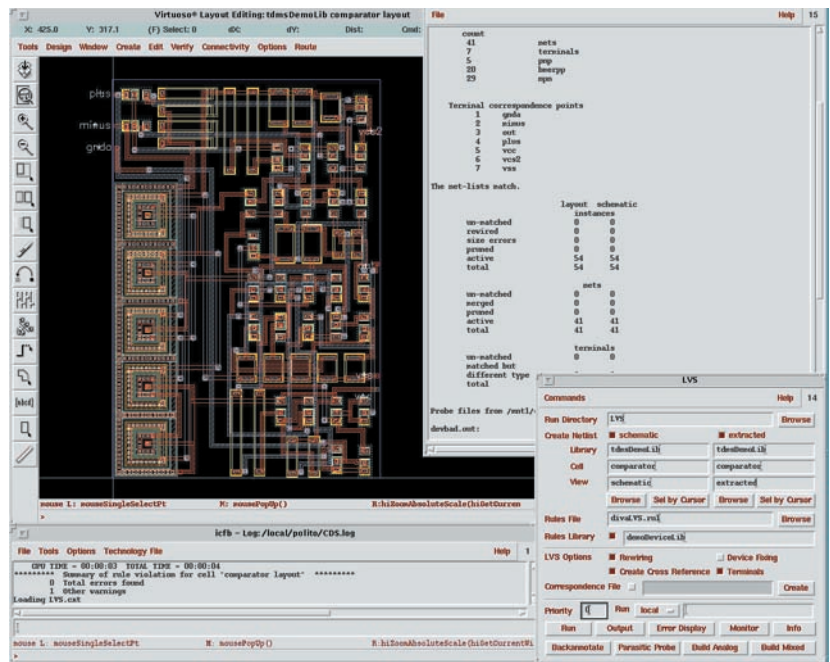


Figure 3: Diva LVS submission form and example LVS summary report

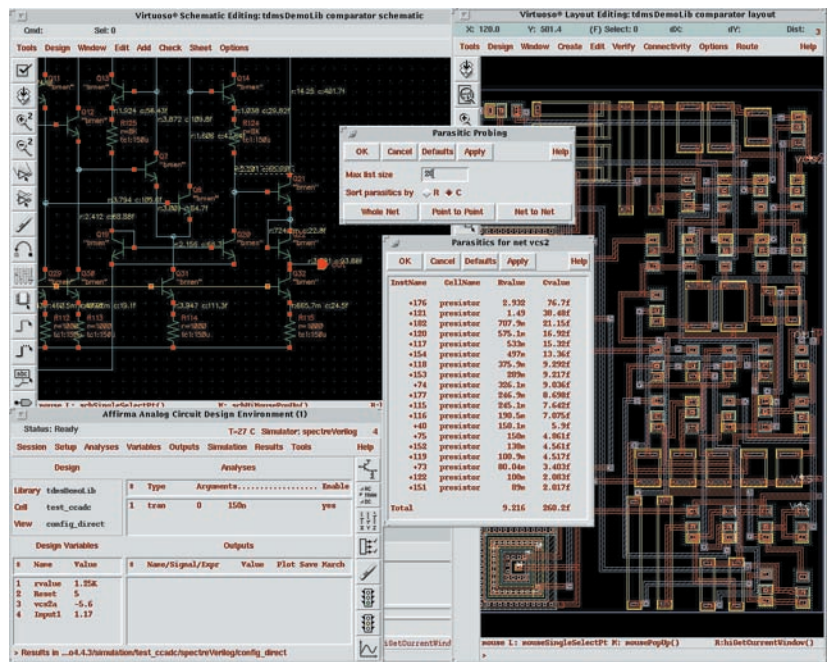


Figure 4: Parasitic probing of Diva RCX results backannotated on the schematic

SPECIFICATIONS

POWERFUL RULE LANGUAGE/SYNTAX

- SKILL-based rules language facilitates complex data manipulations and specialize DRC and LVS rules
- Comprehensive antenna rule syntax supports conjunctive and conditional rules
- All-angle data handling supports all IC process technologies
- User-defined device descriptions support any IC process technology
- User-defined equations provides for accurate device calculations

PERFORMANCE AND CAPACITY

- Incremental DRC operation reduces redundant checking and runtimes
- Support macro-level LVS methodology for faster LVS runtimes
- Consolidation options reduce groups of devices of the same type connected in series or parallel into a single device for comparison
- Intuitive and efficient LVS debugger tools such as the rewire function helps reduce overall verification cycle time

EASE-OF-USE

- Displays online, integrated graphical results for quick analysis
- Tightly integrated with Virtuoso Layout Editor and Virtuoso Analog Design Environment
- Fast error correction using edit-in-place or descend modes within Virtuoso Layout Editor
- Perform XOR comparison between two databases
- Window DRC operation allows fast localized checking, especially useful during chip assembly or for last minute edits to reduce redundant checking and runtimes
- Immediate error and warning messages during interactive sessions via command interpreter window (CIW)
- Access layout data in edit- or read-only modes
- Cross-probing and highlighting eases debugging analysis

DESIGN INPUTS

- Cadence CDBA database (DFII)
- Diva rules

DESIGN OUTPUTS

- Cadence CDBA database (DFII) (layout and extracted)
- Error markers
- Textual reports for debugging and archival purposes

PLATFORMS

- Sun Solaris
- HP-UX
- IBM-AIX
- Linux (Red Hat)

CADENCE SERVICES AND SUPPORT

- Customer-focused solutions that increase ROI, reduce risk, and achieve your design goals faster
 - Collaborative approach and design infrastructure—virtual teaming
 - Proven methodology and flow tuned to your design environment
 - Design and EDA implementation expertise
- Product and flow training to fit your needs and preferred learning style
 - Over 80 instructor-led courses—certified instructors, real world experience
 - More than 25 Internet Learning Series (iLS) online courses
- Cadence customer support that keeps your design team productive
 - Cadence applications engineers provide technical assistance
 - SourceLink® online support gives you access to software updates, technical documentation, and more—24 hours a day, seven days a week

CADENCE PDK AND FOUNDRY SUPPORT

Diva rule files are fully qualified for use with the Cadence Process Design Kits (PDKs), which can be obtained for free from the merchant foundries. These kits are developed and tested by Cadence and supplied to the foundries to support your success in designing chips with particular foundry processes. Please check your merchant foundry web site for the availability of PDK and Diva rule files.

FOR MORE INFORMATION

Email us at info@cadence.com, or log on to www.cadence.com