DATASHEET

CADENCE PCB DESIGN: LAYOUT AND ROUTING

Complex physical and electrical constraints, densely packed components, and faster high-speed technology requirements are just some of the things adding complexity to today's PCB designs. Designers need the ability to easily define, manage, and validate simple physical/spacing constraints—as well as critical high-speed signals—at any stage of the design process. At the same time, they must ensure that the final PCB meets performance, manufacturing, and test specifications goals.

Cadence PCB design solutions are available in the following product suites:

- Cadence Allegro PCB Design L, XL, and GXL and options
- Cadence OrCAD PCB Designer, Cadence OrCAD PCB Designer with PSpice, and Cadence OrCAD PCB Designer Basics
- Cadence OrCAD EE Designer and Cadence OrCAD EE Designer Plus

CADENCE PCB DESIGN SOLUTIONS

Cadence® PCB design solutions are complete design environments for solving and implementing these design challenges and manufacturability concerns. The design solutions contain everything needed to take a PCB design from concept to production with a fully integrated design flow including design capture, component tools, a PCB editor, and an auto/interactive router as well as interfaces for manufacturing, and mechanical CAD. A common database architecture, use model and library offers fully scalable PCB solutions for both Cadence OrCAD® and Allegro® product lines giving you the ability to grow and expand as designs and design challenges increase in complexity. The results are increased productivity, shorter design cycles, and faster ramp up to volume production.

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BENEFITS

- Proven, scalable, cost-effective PCB editing and routing solution that grows as needed
- Provides a complete interconnect environment from basic/advanced floorplanning and routing through strategic planning and global routing
- Speeds advanced designs with high-speed rules/constraints
- Includes a comprehensive feature set

cadence™

- Features a front-to-back constraint management system for constraint creation, management, and validation
- Increases productivity through application integration
- Tight front-to-back integration

FEATURES

PCB EDITOR TECHNOLOGY

PCB EDITING ENVIRONMENT

At the heart of Cadence PCB design solutions is a PCB editor—an intuitive, easy-to-use, constraint-driven environment for creating and editing simple to complex PCBs. Its extensive feature set addresses a wide range of today's design and manufacturability challenges. The PCB editor provides a powerful and flexible set of floorplanning tools. PCB design partitioning technology, in the Allegro tiers, provides a concurrent design methodology for faster time to market and reduced layout time. Powerful shape-based shove/hug interactive etch creation/editing provides a highly productive interconnect environment while providing real-time, heads-up displays of length and timing margins. Dynamic shape capability offers real-time copper pour plowing/healing functionality during placement and routing iterations. The PCB editor can also generate a full suite of phototooling, bare-board fabrication and test outputs, including Gerber 274x, NC drill, and bare-board test in a variety of formats. *(See Figure 1.)*

CONSTRAINT MANAGEMENT

A constraint management system displays physical/spacing and high-speed rules along with their status (based on the current state of the design) in real time and is available at all stages of the design process. Each worksheet provides a spreadsheet interface that enables the user to define, manage, and validate the different rules in a hierarchical fashion. This powerful application allows designers to graphically create, edit, and review constraint sets as graphical topologies that act as electronic blueprints of an ideal implementation strategy. Once the constraints are present in the database, they are used to drive the placement and routing processes for constrained signals. The constraint management system is completely integrated with the PCB editor and constraints can be validated in real time as the design process proceeds. The results of the validation process is a graphical representation of constraint pass or fail highlighted as green for passing or red for failures. This allows designers to immediately see the progress of the design as well as the impact of any design changes in the spreadsheets.

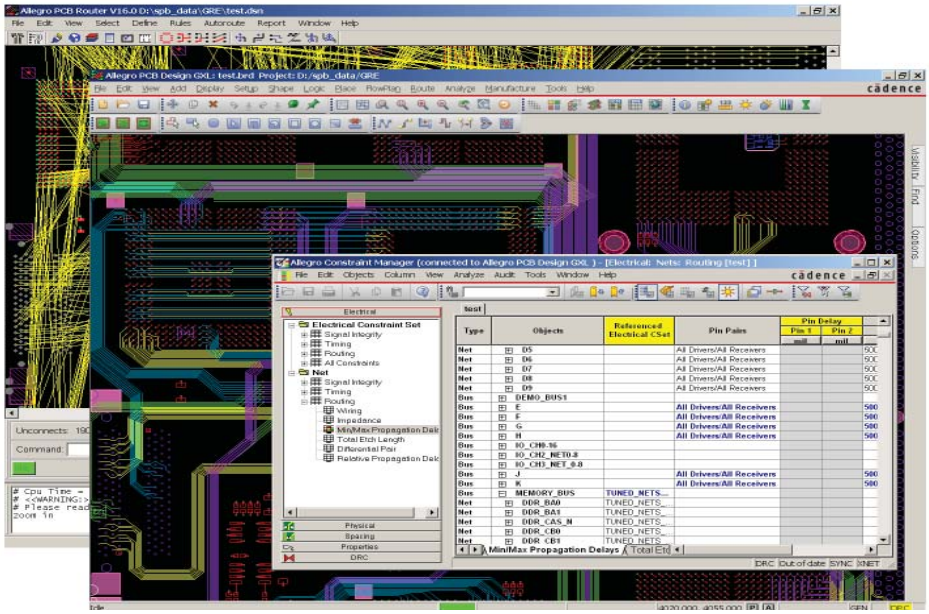

Figure 1: Cadence PCB design solutions bring together all the tools needed to design simple-to-complex PCBs

FLOORPLANNING AND PLACEMENT

The constraint and rules-driven methodology drives a powerful and flexible set of placement capabilities, including interactive and automatic component placement. The engineer or designer can assign components or subcircuits to specific "rooms" during design entry or floorplanning. Components can be filtered and selected by reference designator, device package/footprint style, associated net name, part number, or the schematic sheet/page number. With thousands of components on today's boards, needing precise management, real-time assembly analysis and feedback increases the designer's productivity and efficiency by placing components to corporate or EMS guidelines. Design-for-assembly (DFA) analysis (available in the Allegro PCB Design XL and GXL tiers) offers this real-time package-to-package clearance checking during interactive component placement. Driven from a two-dimensional spreadsheet array of classes and package instances, real-time feedback provides minimum clearance requirements based on the package's side-to-side, side-to-end, or end-to-end profiles. As a result, the PCB designer can simultaneously place devices for optimum routability, manufacturability, and signal timing.

STRATEGIC PLANNING AND DESIGN INTENT

Highly constrained, high-density designs dominated by bussed interconnect can take significant time to strategically plan and route. Compound this with the density issues of today's components, new signaling levels, and specific topology requirements, traditional CAD tools and technologies fall short of being able to capture a designer's specific routing intent and act upon it. The Global Route

Environment technology (available only in Allegro PCB Design GXL) provides the technology and methodology to capture as well as adhere to a designer's intent. Through the interconnect flow planning architecture and the global route engine, users can for the first time put their experience and design intent into a tool that understands what they want—natively.

The solution accomplishes this by allowing the user to create abstracted interconnect data (through the interconnect flow planning architecture) and quickly converge on a solution and validate it with the global route engine. Use of interconnect abstraction reduces the number of elements the system has to deal with. Reducing the number of elements from potentially tens of thousands of elements down to hundreds results in a significant reduction in the amount of manual interaction required. Additionally, it reduces the number of visual elements the user sees in the interconnect flow planning architecture, decreasing the number of elements they must physically manage. Using the abstract data, the planning and routing process can be accelerated by providing a visual/spatial map of the open area in relation to the abstract data and users design intent. The route engine can then deal with the details of the routing, adhering to the specified intent, without the user having to both visualize and solve the interconnect problems at the same time. This represents a significant simplification over current design tools allowing users to get their designs completed faster and more efficiently. Users can now converge on a successful interconnect solution far faster and more easily than ever before, reducing design cycle time through increased efficiency and productivity. *(See Figure 2.)*

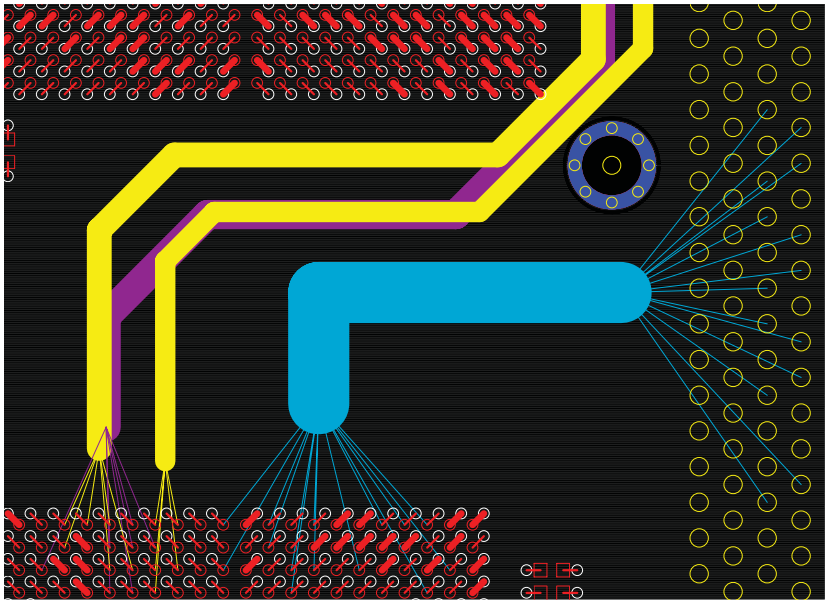

Figure 2: Interconnect flow planning allows users to create abstracted interconnect data and quickly converge on a solution and validate it with the global route engine

DESIGN PARTITIONING

The increasing deployment of globally dispersed design teams compounds the problems associated with trying to shorten design cycle times. Manual workarounds that address multi-user challenges are time consuming, slow and prone to error. PCB design partitioning technology (available in the Allegro PCB design tiers) provides a multi-user, concurrent design methodology for faster time to market and reduction in layout time. Using this technology, multiple designers working concurrently on a layout share access to a single database, regardless of team proximity. Design partitioning technology allows designers to partition designs into multiple sections or areas for layout and editing by several design team members. As a result, each designer can view all partitioned sections and update the design view for monitoring the status and progress of other users' sections. This can dramatically reduce overall design cycles and accelerate the design process.

INTERACTIVE ETCH EDITING

The interactive routing capability of the PCB editor provides powerful, interactive features that deliver controlled automation to maintain user control, while maximizing routing productivity. Real-time, shape-based, any angle, push/shove routing enables users to choose between "shove-preferred," "hug-preferred," or "hug-only" modes. Shove-preferred mode allows users to construct the optimum interconnect path while the real-time, shape-based router takes care of dynamically pushing obstacles. Routes will automatically jump over obstacles such as pins or vias. The hug-preferred mode is the perfect solution when a databus needs to be constructed. In hug-preferred mode, the router contour follows other interconnect as a priority and only pushes aside or jumps obstacles when there is no other option. The hug-only option performs like the hug-preferred mode, but without the push-and-shove aggression on other etch objects. The real-time, embedded, shape-based routing engine optimizes the route by either pushing obstacles or contour-following obstacles while dynamically jumping vias or component pins.

During etch editing, the designer is provided with a real-time, graphical heads-up display that shows how much timing slack remains for interconnect that has high-speed constraints. Interactive routing also provides the ability to perform group routing on multiple nets and interactive tuning of nets with high-speed length or delay constraints. *(See Figure 3.)*

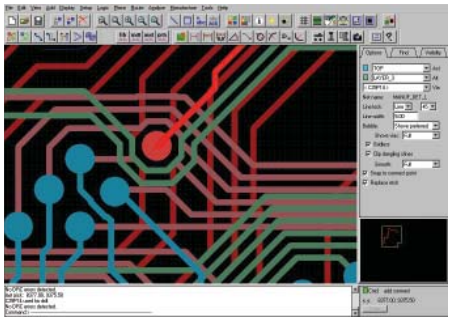

Figure 3: Dynamic push-and-shove capabilities make interactive editing easy on even the most advanced designs

DYNAMIC SHAPES

Dynamic shape technology offers real-time copper pour plowing/healing functionality. Shape parameters can be applied at three different levels. Parameters are structured into global, shape instance, and object-level hierarchies. Traces, vias, and components added to a dynamic shape will automatically plow and void through the shape. When items are removed, the shape will automatically fill back in. Dynamic shapes do not require batch autovoiding or other post-processing steps after edits are made.

RF DESIGN

Design requirements involving high-performance/high-frequency circuits need to be solved faster and more accurately than ever before. The RF/mixed signal technology provides a complete, front-to-back solution from schematic to layout and manufacturing for PCB RF design. RF technology includes advanced RF capabilities, including intelligent layout functionality for parametrically creating and editing RF geometries and a flexible shape editor. A bi-directional IFF interface provides quick and efficient transfer of RF circuit data for simulation and validation. This bi-directional flow eliminates the manual and error-prone iterations between circuit simulation and layout. (This feature is available in Allegro PCB Design XL and GXL-level tiers). *(See Figure 4.)*

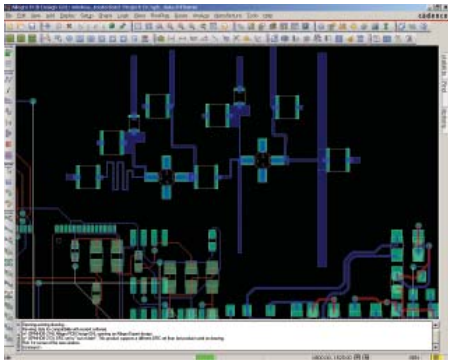

Figure 4: Complete front-to-back solution for PCB RF design

PCB MANUFACTURING

A full suite of photo-tooling, bare-board fabrication and test outputs, including Gerber 274x, NC drill, and bare-board test in a variety of formats can be generated. More importantly, Cadence supports the industry initiative towards Gerber-less manufacturing through its Valor ODB++ interface that also includes the Valor Universal Viewer. The ODB++ data format creates accurate and reliable manufacturing data for high-quality, Gerber-less manufacturing.

PCB AUTOROUTER TECHNOLOGY

AUTOMATED INTERCONNECT ENVIRONMENT

Increased design complexity, density, and high-speed routing constraints make manual routing of PCBs difficult as well as time-consuming. The challenges of complex interconnect routing are solved with powerful, automated technology. This robust, production-proven autorouter includes a batch routing mode with extensive user-defined routing strategy control as well as built-in automatic strategy capability. An interactive routing environment—that features real-time interactive trace pushing and shoving—aids in making quick edits to traces. An interactive placement environment with extensive floorplanning functionality and complete component placement features eliminates the need to switch applications to make placement changes to optimize routing. By using the auto-interactive floorplanning and placement capability, designers can improve routing quality and productivity, which are directly related to component placement. In addition, an extensive rule set allows designers to control a wide range of constraints from default board-level rules to rules by net/net class, and regions rules. High-speed routing features, available in the Allegro product tiers, provides capabilities to handle the net scheduling, timing, crosstalk, layer set routing, and special geometry requirements demanded by today's high-speed circuits.

AUTOROUTNG

Advanced autorouting technology provides powerful, shape-based autorouting with fast, high completion rates. Its routing algorithms are designed to handle a wide range of PCB interconnect challenges—from simple to complex, low density to high density—as well as the demands of high-speed constraints. These powerful algorithms make the most efficient use of the routing area. To find the best routing solution for each case, the router uses a multi-pass, cost-based, conflict resolution algorithms. An extensive rule set provides the capability for physical and electrical constraint control. The extensive rule set has the flexibility to handle specific rules on various routing elements in a design. Users can define rules required to meet common physical/spacing net rules and class rules to complex, hierarchical high-speed rules. *(See Figure 5.)*

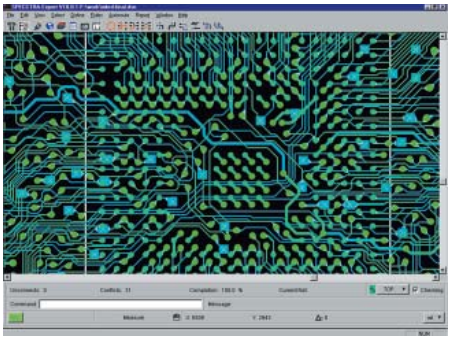

Figure 5: Advanced autorouting technology effectively handles dense, highly constrained designs

DESIGN FOR MANUFACTURING

The design for manufacturing capability significantly improves manufacturing yields. Manufacturing algorithms provide spreading capability that automatically increases conductor clearances on a space available basis. Automatic conductor spreading is used to improve manufacturability by repositioning conductors to create extra space between: conductors and pins, conductors and SMD pads, and adjacent conductor segments. Users have the flexibility to define a range of spacing values or to use the default values. Mitered corners and test points can be added throughout the routing process. The manufacturing algorithms automatically use the optimal setback range, starting from the largest to the smallest value. Test point insertion automatically adds testable vias or pads as test points. Testable vias can be probed on the front, back, or both sides of the PCB, supporting both single side and clamshell testers. Designers have the flexibility to select the test point insertion methodology that conforms to their manufacturing requirements. Test points can be "fixed" to avoid costly test fixture modifications. Test point constraints include test probe surfaces, via sizes, via grids, and minimum center-to-center distance.

INTERACTIVE ROUTE EDITING

A route editor simplifies and streamlines the etch editing process. As new conductors arerouted, the plowing feature automatically pushes aside existing conductors and routes around pins. Using the shoving feature, designers can move conductor segments or vias against existing traces and push ahead over other pins and vias if necessary. A ghosting feature makes it easy to evaluate "what if" scenarios. As a conductor segment or via is moved under cursor control, the surrounding conductor is shoved and displayed dynamically so the adjusted routing can be evaluated before accepting a final configuration. The route editor is ideal for dense, multilayer boards where legal via sites can be difficult to find. Vias are positioned by simply clicking twice at a chosen location. If possible, the chosen site is made available by shoving conductors aside on layers as needed. If not, the route editor displays a design rule violation and shows the legal via sites nearby. In addition, the copyroute feature, which allows an existing route to be copied to complete unrouted bus connections, simplifies bus construction.

PLACEMENT EDITING

The placement editor allows designers to quickly place components while simultaneously evaluating space, logic flow, and congestion before beginning the route or as needed during the routing process PCB. The Move mode allows components to be flipped, rotated, aligned, pushed, and moved either as individual components or as a group. The Guided-Place mode selects the component with the highest connectivity and computes an optimal placement location that does not violate design rules or constraints. The location can be accepted or rejected by the user. Components can be placed by directly entering their X-Y locations. This capability is particularly useful for placing connectors and components with fixed locations. Density analysis graphically displays circuit congestion by overlaying the PCB with a color map showing a range of areas—from highly congested areas to lightly congested. This helps determine where placement adjustments could be made to relieve congestion and improve routing completion. *(See Figure 6.)*

HIGH-SPEED CONSTRAINTS

High-speed routing constraints and algorithms handle differential pairs, net scheduling, timing, crosstalk, layer set routing, and the special geometry requirements demanded by today's high-speed circuits. For differential pair routing, users define the gap between the two conductors and the autorouter takes care of the rest. The routing algorithms intelligently handle routing around or through vias, and automatically conforms to defined length or timing criteria. Automatic net shielding is used to reduce noise on noise-sensitive nets. Separate design rules may be applied to different regions of the design. For example, users can specify tight clearance rules in the connector area of a design and less stringent rules elsewhere.

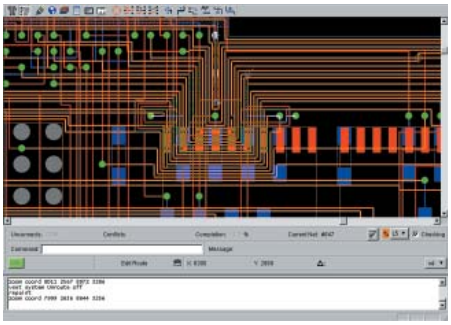

Figure 6: Placement Editor allows you to evaluate space, logic flow, and congestion at all stages of the routing process

PCB EDITOR INTEGRATION

The PCB routing technologies are tightly integrated with the PCB editor. Through the PCB editor interface, all design information and constraints are automatically passed to the router. Once the route is completed, all route information is automatically passed back to the PCB editor.

DOCUMENTATION

Cadence tools provide an extensive set of documentation, which includes user guides, context-sensitive help (F1), reference guides, online tutorial, and multimedia demonstrations.

The documentation set helps you to:

- Find the answer you need by searching the online help system and navigate quickly between related topics with extensive hypertext cross-references
- Learn the tool with the help of the online interactive tutorial
- Find information on error and warning scenarios

OPERATING SYSTEM SUPPORT

Allegro platform technology:

- Sun Solaris
- Linux
- IBM AIX
- Windows

OrCAD technology:

- Windows

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

PCB EDITOR FEATURE SUMMARY	OrCAD PCB DESIGNER/BASICS	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Limited database (layers, components, connections)	Basics	n/a	n/a	n/a
Unlimited database	Designer	•	•	•
Netlist/crossplace/crossprobe	•	•	•	•
Padstack and symbol editor	•	•	•	•
Customizable/automated drill legend/NC output	•	•	•	•
Multiple via sizes, blind/buried via support	•	•	•	•
Autoplacement/Quickplace/Floorplanner	•	•	•	•
Dynamic shapes with real-time plowing and healing	•	•	•	•
2-D drafting and dimensioning	•	•	•	•
Gerber 274X, 274D artwork output generation	•	•	•	•
Multiple UNDO/REDO	•	•	•	•
Valor ODB++, ODB++(X) and universal viewer	•	•	•	•
HTML-based reports	•	•	•	•
Exposed copper DRC	•	•	•	•
Interactive routing/etch editing	•	•	•	•
Automatic silkscreen generation	•	•	•	•
Split plane support	•	•	•	•
SKILL runtime, macro, and script support	•	•	•	•
Variant Editor (Design Entry HDL)	n/a	•	•	•
Variant assembly drawing creation	•	•	•	•
Variant bill-of-materials generation	•	•	•	•
IFF import	•	•	•	•
CAD interfaces – DXF (Ver.14), IDF (Ver. 2 and 3)	•	•	•	•
PCB interfaces – PADS (Ver.5), P-CAD (Ver.8), OrCAD Layout	•	•	•	•
Constraint manager (physical, spacing, properties, and DRC)	•	•	•	•
Manual testprep	•	•	•	•
Length, parallelism, and differential pairs rule support		PCB Performance Option	•	•
Pin-pair multi/matched nested group support		PCB Performance Option	•	•
Real-time DRC and routing of differential pairs and length rules		PCB Performance Option	•	•
Interactive delay tuning		PCB Performance Option	•	•
Complex physical design rule checking (no electrical)		PCB Performance Option	•	•
Group routing		PCB Performance Option	•	•
Measure parasitic		PCB Performance Option	•	•
Advanced trace glossing		PCB Performance Option	•	•
Database-driven design reuse modules		PCB Performance Option	•	•
Technology files		PCB Performance Option	•	•
Design-for-assembly rule checking		PCB Performance Option	•	•

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

PCB EDITOR FEATURE SUMMARY	OrCAD PCB DESIGNER/BASICS	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Automatic testprep		PCB Performance Option	•	•
Constraint manager (physical, spacing, electrical (routing), properties and DRC)		PCB Performance Option	•	•
Allegro PCB Router high-speed routing alignment (6U)		PCB Performance Option	•	•
Real-time DRC of delay and crosstalk rules		PCB Performance Option	•	•
Constraint regions and technology file support		PCB Performance Option	•	•
Automatic line width adjustment for impedance rules		PCB Performance Option	•	•
eXtended net support (x-nets)		PCB Performance Option	•	•
Layer set rules and routing support		PCB Performance Option	•	•
Via array/shielding		PCB Performance Option	•	•
SKILL development		PCB Performance Option	•	•
Delay, crosstalk, and impedance routing support			•	•
Constraint manager (physical, spacing, electrical (all), properties and DRC)			•	•
Z-axis delay support			•	•
Extended timing path support			•	•
Group routing (space control)			•	•
Dynamic phase control for differential pairs			•	•
Dynamic design-for-assembly analysis (real-time feedback)			•	•
Display and spread segments over voids			•	•
Back-drilling support			•	•
Hierarchical flow planning				•
Interconnect data abstraction				•
Global route engine				•
PCB design partitioning technology		PCB Partitioning Option*	PCB Partitioning Option	PCB Partitioning Option
Bi-directional IFF interface			PCB RF Option	PCB RF Option
RF geometry and circuit creation/editing			PCB RF Option	PCB RF Option

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

PCB ROUTER FEATURE SUMMARY	OrCAD PCB DESIGNER/ BASICS***	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
6 signal layer limit	•	•	n/a	n/a
256 signal layer limit	n/a	Router Auto/ Interactive Option	•	•
Shape-based or gridded autorouting	•	•	•	•
SMD fanout	•	•	•	•
Trace width by net and net classes	•	•	•	•

*PCB Performance Option required

*** No PCB Router technology is included in the OrCAD PCB Designer Basics suite

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

PCB ROUTER FEATURE SUMMARY	OrCAD PCB DESIGNER/ BASICS***	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Staggered pin support	•	•	•	•
45-degree ECO routing	•	•	•	•
Memory pattern routing (SMD or through-hole)	•	•	•	•
Interactive via search	•	•	•	•
Interactive routing with shoving and plowing	•	•	•	•
Interactive floorplanning	•	•	•	•
Autoplacement	n/a	n/a	•	•
Online design rule checking	•	•	•	•
Flip, rotate, align, push, and move components	•	•	•	•
Placement density analysis	•	•	•	•
Router support for PCB design partitioning files	n/a	•	•	•
Allegro PCB Router ADV 6U or 256U		Router Performance Option**	•	•
Layer set rules and routing support		Router Performance Option**	•	•
Signals on specific layers		Router Performance Option**	•	•
Width and clearance rules by layer		Router Performance Option**	•	•
Via rules by net and/or net class		Router Performance Option**	•	•
Net and/or net class rules by layer		Router Performance Option**	•	•
Crosstalk violation report		Router Performance Option**	•	•
Trace length violation report		Router Performance Option**	•	•
Blind and buried via support		Router Performance Option**	•	•
Via under SMD pad checking		Router Performance Option**	•	•
Automatic wire bonding		Router Performance Option**	•	•
Plural vias		Router Performance Option**	•	•
Stacked vias		Router Performance Option**	•	•
Enhanced via fanout		Router Performance Option**	•	•
Allegro PCB Router DFM 6U or 256U		Router Performance Option**	•	•
Automatic trace spreading		Router Performance Option**	•	•
Automatic via reduction		Router Performance Option**	•	•
Automatic miter 90 to 45		Router Performance Option**	•	•
Automatic test point generation		Router Performance Option**	•	•
Test point specific clearance rules		Router Performance Option**	•	•

*PCB Performance Option required

** Router Auto/Interactive required

*** No PCB Router technology is included in the OrCAD PCB Designer Basics suite

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

PCB ROUTER FEATURE SUMMARY	OrCAD PCB DESIGNER/ BASICS***	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Allegro PCB Router HP 6U or 256U		PCB Perfomance Option	•	•
Minimum, maximum, and matched length rules		PCB Perfomance Option	•	•
Crosstalk controls on same and adjacent layers		PCB Perfomance Option	•	•
Virtual pins, which can be moved during autorouting		PCB Perfomance Option	•	•
Parallelism controlled by length and gap		PCB Perfomance Option	•	•
Differential pair routing		PCB Perfomance Option	•	•
Automatic net shielding		PCB Perfomance Option	•	•
Design rules by area		PCB Perfomance Option	•	•
Online display of length tolerance		PCB Perfomance Option	•	•
Global violation indicator		PCB Perfomance Option	•	•
Dynamic display of available length		PCB Perfomance Option	•	•
Automatic single net routing		PCB Perfomance Option	•	•
Multiple net/bus routing		PCB Perfomance Option	•	•
Relative delay rules		PCB Perfomance Option	•	•
Z-Axis delay support (PCB Editor integration)		PCB Perfomance Option	•	•
Extended timing path support (PCB Editor integration)		PCB Perfomance Option	•	•
Pin-pair multi/matched nested group support (PCB Editor integration)		PCB Perfomance Option	•	•

PCB DESIGN SOLUTIONS COMPARISON GRID
OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

FRONT-END OPTIONS SUMMARY	OrCAD PCB DESIGNER/BASICS	ALLEGRO PCB DESIGN L	ALLEGRO PCB DESIGN XL	ALLEGRO PCB DESIGN GXL
Allegro Design Entry HDL-or-Allegro Design Entry CIS	OrCAD Capture	•	•	•
Constraint Manager (Allegro Design Entry HDL only)	n/a	n/a	•	•
Part Developer/Component Management	CIS Option	•	•	•
Allegro Design Entry HDL Rules Checker	n/a	n/a	•	•

*** No PCB Router technology is included in the OrCAD PCB Designer Basics suite

For more information about this and other products contact:

1.800.746.6223

or log on to:

www.cadence.com/contact_us

cadence™

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