

CADENCE PHYSICAL VERIFICATION SYSTEM

Proven on many successful production tapeouts in nanometer process technologies, the Cadence® Physical Verification System (PVS) is the premier Cadence solution for SoC signoff. It offers competitive single-processor and distributed processor performance, sufficient for high-end SoC designs implemented in advanced processes. In addition, 100% file compatibility and ease of use make it a drop-in replacement for existing physical verification technologies.

The Cadence Physical Verification System delivers integration with industry-standard digital and custom design flows, enabling designers to procure a front-to-back design and signoff flow from a single EDA vendor. PVS also facilitates a “one tool, one deck” model for digital and custom design that minimizes support overhead. The solution further offers a unique operation-based distributed processing capability that greatly accelerates throughput without requiring specialized hardware.

BENEFITS

- Single-vendor solution for implementation and back-end signoff
- Rapid design turnaround with production-proven accuracy
- Simplifies migration through direct compatibility with industry-standard formats

- Enables “one tool, one deck” model for SoC (custom and digital) design
- Accelerates debug cycle through integration with the Cadence Virtuoso and Encounter platforms
- Runs on cost-effective parallel computing systems with no need for hardware modifications

FEATURES

COMPETITIVE PERFORMANCE MAINTAINS DESIGN THROUGHPUT


PVS delivers single-processor performance that is highly competitive with other industry-leading physical verification solutions. Large designs can also take advantage of the unique operation-based distributed processing architecture that leverages low-cost, off-the-shelf compute platforms to greatly accelerate design throughput.

DROP-IN COMPATIBILITY WITH INDUSTRY-STANDARD FORMATS EASES ADOPTION

All PVS rule files and output files are 100% compatible with industry-standard formats. This allows PVS users to leverage their existing investment in rule decks and infrastructure with no requirement for translation or scripts. Rule decks execute natively on PVS, and PVS reports design errors in an intuitive, predictable and familiar way, which greatly accelerates tool and flow validation and integration.

INTEGRATION WITH ENCOUNTER AND VIRTUOSO PLATFORMS ACCELERATES DESIGN DEBUG

PVS is seamlessly integrated with the Cadence Encounter® digital design platform and the Virtuoso® custom design platform. It also operates in CDB and Open Access environments. This means designers can invoke PVS and browse PVS error markers without leaving their Cadence design environment. PVS also runs stand-alone in batch mode, and supports Cadence QRC parasitic extraction flows.



PVS features the industry's first Verilog®-compatible netlist-based LVS debug capability. An interface with a high-performance, high-capacity design viewer enables PVS users to efficiently debug very large SoC designs with design file sizes in the tens of gigabytes range. PVS also integrates seamlessly with Cadence MaskCompose automated reticle design products.



For more information:
info@cadence.com
sales@cadence.com
www.cadence.com

RAPID TURNAROUND WITH PRODUCTION-PROVEN ACCURACY

PVS is production-proven, with multiple successful customer tapeouts in advanced nanometer process technologies from multiple foundries.

cadence™

Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS

2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 (*within US*)
+1.408.943.1234 (*outside US*)
F: +1.408.943.5001
www.cadence.com