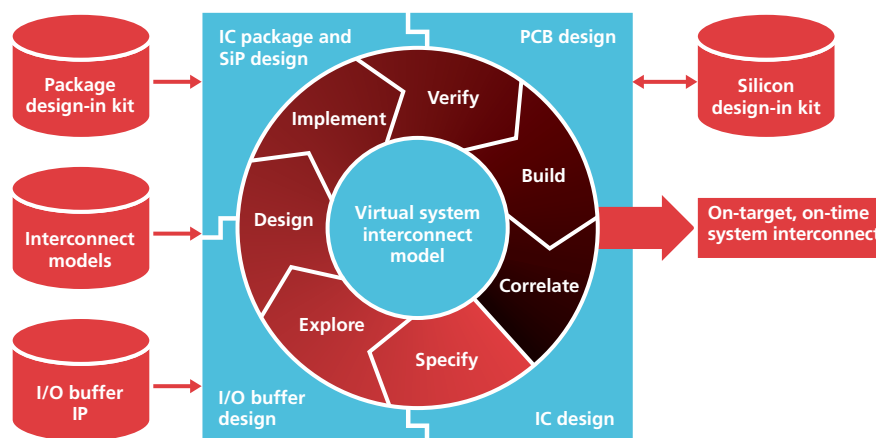


## CADENCE 3D DESIGN VIEWER

Cadence® 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond design rule checking (DRC) solution for complex IC package designs. Tightly integrated with Allegro® Package Designer L and Allegro Package Designer XL, it allows users to visualize, investigate, and wirebond DRC check an entire design, or selected design subset, reducing design cycle time and improving product manufacturability.



*The Allegro system interconnect design platform*

### THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect—between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The Allegro constraint-driven flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With silicon design-in kits, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter™ and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.

## AN INTELLIGENT 3D DESIGN VIEW

Virtually all of today's EDA tools for fabric physical layout — IC, IC package, or PCB — are two-dimensional. While ideal for substrate layout, interconnect planning, metal fill creation and the like this “plan-view” process does not lend itself well to the design, management, and verification of complex die stack towers. The design complexity and density involved require a more realistic approach.

The Cadence 3D Design Viewer meets this need by providing an IC package designer with the capability to physically visualize a design as it will actually look during manufacture. A designer can interactively zoom, pan, and rotate the 3D view as well as select from a set of predefined views.

## EMBEDDED WITH IC PACKAGE LAYOUT

The 3D Viewer can be accessed from either the Allegro Package Designer L or Allegro Package Designer XL user interface. When invoking the “3D View” the designer is presented with a substrate stackup dialog so verification of the current design can be performed prior to the creation of the design's 3D model. If a package design contains a die stack, the vertical (Z-dimension) information for the die(s) and any spacers/interposers need to be entered in the stackup dialog prior to generation of the 3D model. At this time, the designer can also specify package ball dimensions, colors and multiple wire profiles (four- and five- point models) as well as multiple 3D wirebond DRC rules.

The benefits of working with the third dimension are clear when the same design is viewed in 2D and then in 3D. For demonstration purposes a fairly simple design is used — a single two-die stack on a ball grid array (BGA) substrate. The base die is flip-chip attached; the top die is wirebond attached. In the 2D editor view (Figure 1), visualizing and validating the die stack and the wirebond ring is challenging, even for a seasoned package designer. And, due to the complexity, it would be almost

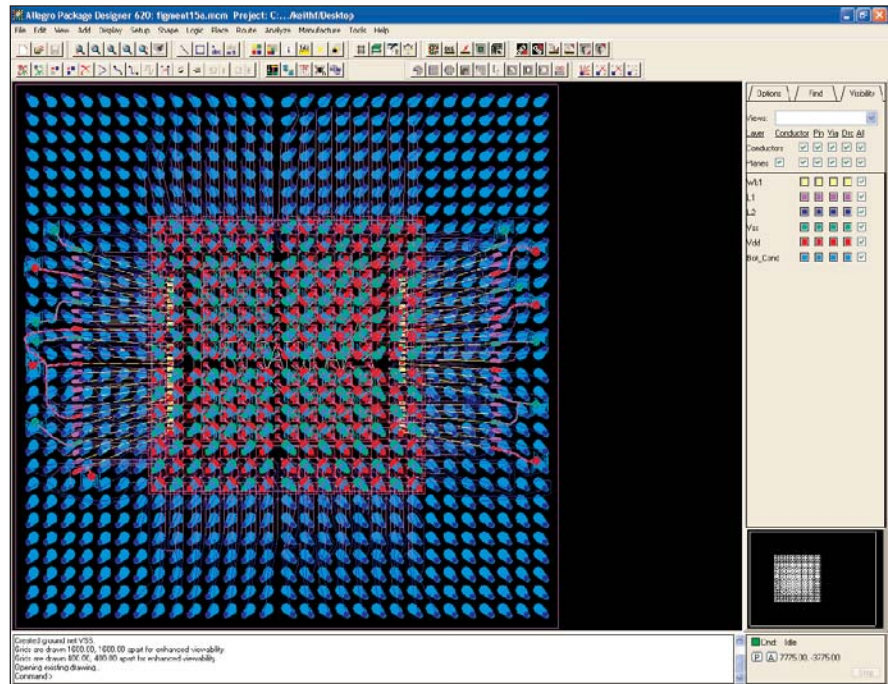


Figure 1: Single stack of two die on a BGA substrate viewed in Allegro Package Designer with a 2D viewer

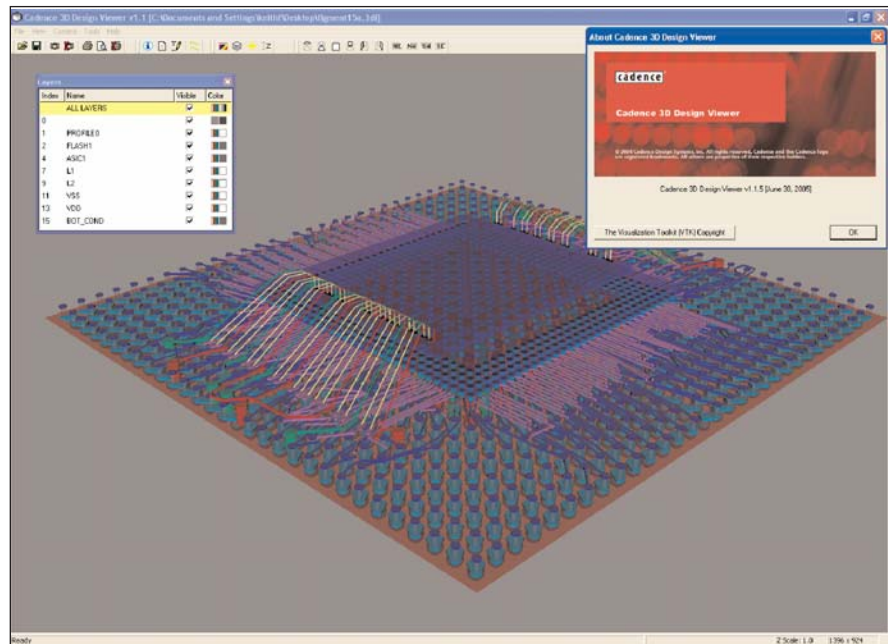


Figure 2: Cadence 3D Design Viewer lets users visualize the design as it will actually look

impossible to hold a design review with an architect or lead engineer.

When the same design is loaded into the 3D Design Viewer (Figure 2) the designer and the engineering team can not only easily visualize,

investigate, and create collaborative markups but they can also perform detailed 3D wirebond checking, including the ability to define, modify, and assign new wirebond profiles.

## EASY DESIGN INVESTIGATION

Cross referencing is easy as the 3D Design Viewer uses the same color/layer/object settings as defined in Allegro Package Designer. Layer visualization can be turned on/off and layer transparency set. For detailed design investigation, the 3D Viewer has similar “show element” information command capability that can be used by “object” or by “net.” Importantly, the user has control over the highlight color and the level of transparency applied to none selected objects.

The 3D Viewer is especially effective when trying to understand and visualize complex via arrays, especially on designs using build-up layers. *Figure 3* illustrates how difficult it is to understand the connectivity path of the differential pair between the metal interconnect and the package substrate ball when viewed in 2D.

Contrast this figure with the 3D view of the same differential pair. The designer can easily visualize the via arrays and interconnect path from the differential pair to substrate balls.

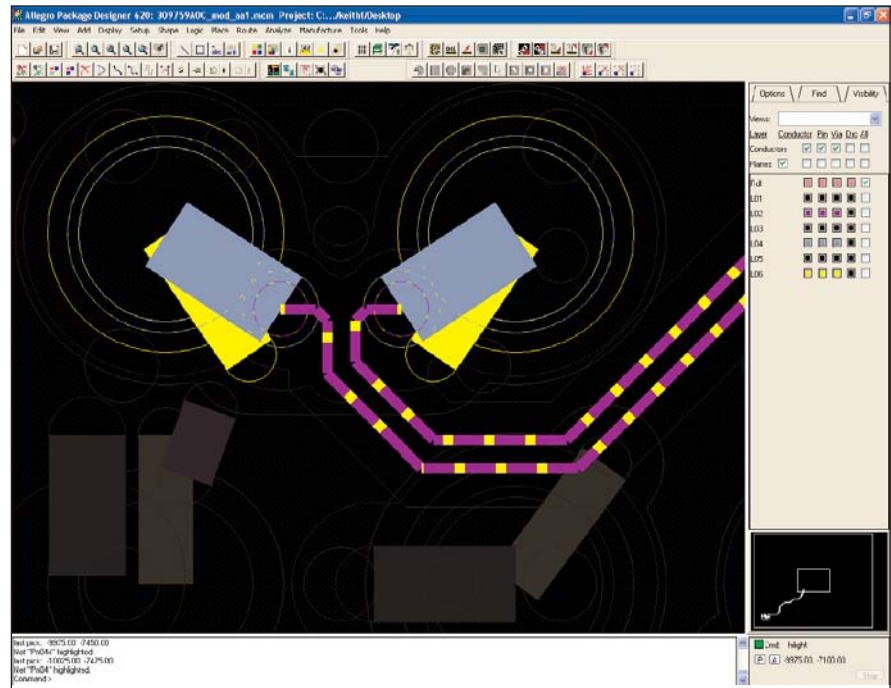
## INTERACTIVE MARKUP

During 3D design viewing an engineer can create “markup” jpeg snapshots for design reviews and/or design documentation that include the ability to add basic shapes, arrows and text. This is especially useful for communications with the design chain partners and test and assembly manufacturing departments.

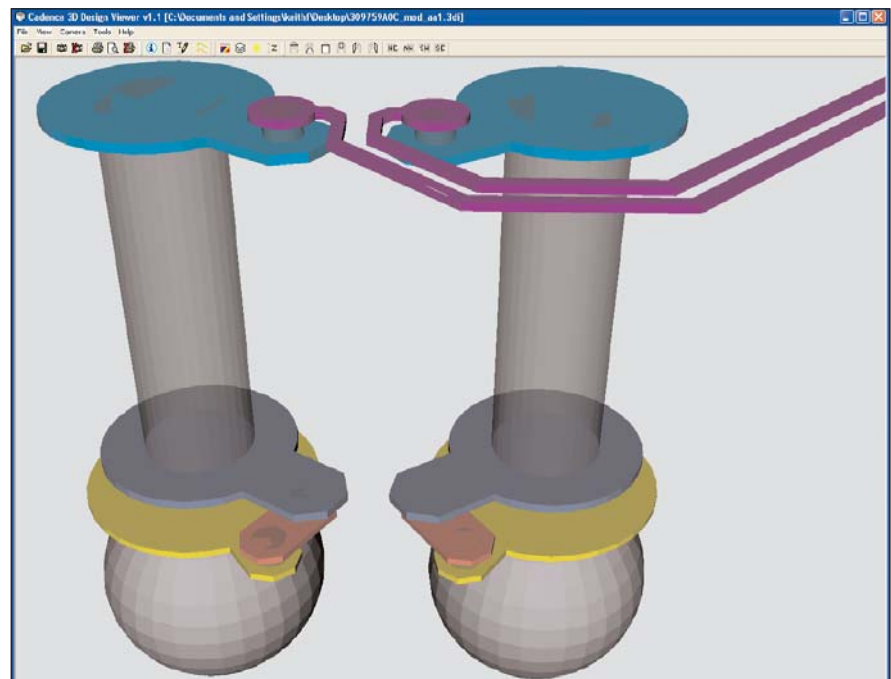
## 3D WIREBOND CLEARANCE DESIGN RULE CHECKING

Rules are defined and stored as part of the Allegro Package Designer design session. Completely user-defined, they can be used to check the following 3D clearances:

- All signals to all signals, all signals to named signal, or named signal to named signal
- Bondwire to bondwire same bond tier or tier ‘n’ to tier ‘n’
- Bondwire to bondfinger same bond tier or tier ‘n’ to tier ‘n’
- Bondwire to metal route, metal filled shape or die/spacer body on the same layer, or any adjacent layer



*Figure 3: It is difficult to understand the connectivity path between the metal interconnect and the package substrate ball in a 2D view*



*Figure 4: In a 3D view a designer can precisely visualize the via arrays and interconnect path from the differential pair to substrate balls*

*Figure 5* shows how the 3D Viewer enhances the designers debug capability—the “info” command highlights the DRC marker and the

associated wirebonds as well as indicating the rule, rule value, and actual value.

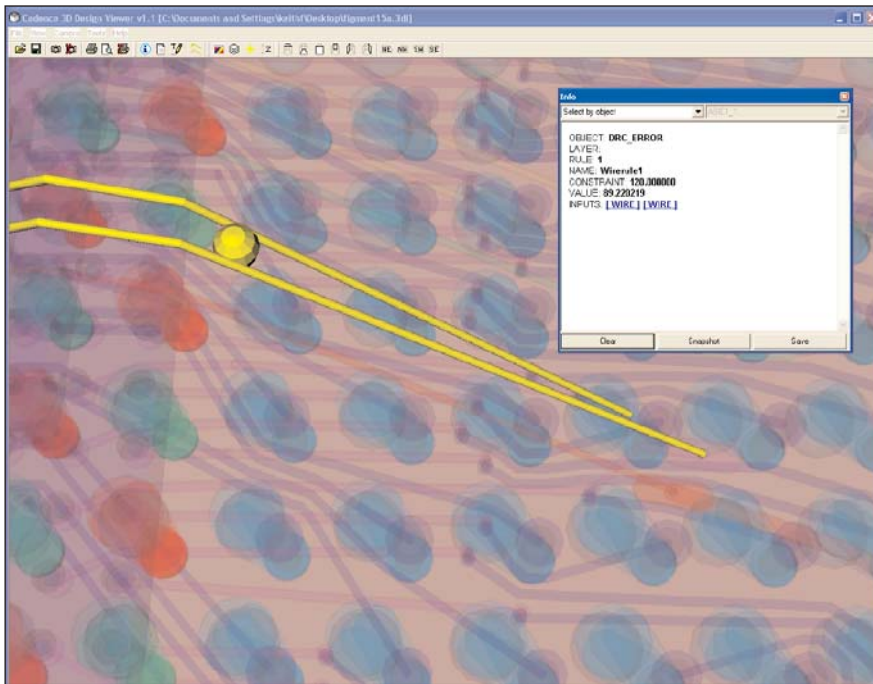


Figure 5: Highlighting the DRC using the “info” command

## OPERATING SYSTEM SUPPORT

- Windows 2000 with Service Pack 4, XP Professional
- OpenGL compliant graphics card with a minimum of 64MB of dedicated memory

## CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

## FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223 or visit [www.cadence.com](http://www.cadence.com) for additional information. To locate a Cadence sales office or value-added reseller (VAR) in your area, visit [www.cadence.com/contact\\_us](http://www.cadence.com/contact_us).