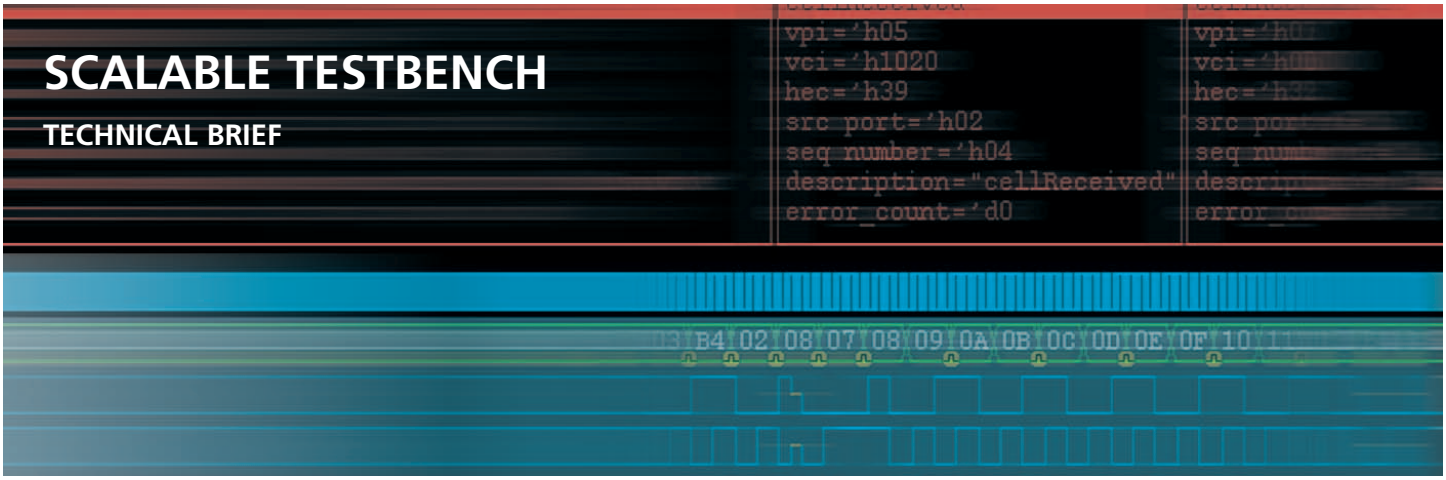
cadence

SCALABLE TESTBENCH

TECHNICAL BRIEF



INCISIVE TECHNICAL BRIEFS	
▶ Scalable performance	Palladium + Xtreme
▶ Total reuse	*e*VC, *e*RM, vPlan
▶ Verification IP	
▶ Verification management	Incisive management
▶ Mixed-language	Viewports
▼ Scalable testbench	Specman Elite + Incisive simulation

— Scaling up to full-chip and system-level verification
— Unique advantages of system-level verification technology
  – Abstract layered sequences and multi-channel stimulus generation
  – Support for heterogeneous verification environments
  – Scalable constraint solver and stimulus generator
  – Scalable coverage engine
  – System-level debugging
  – Testbench interfaces to multiple system-level representations
  – Verification IP reuse and system-level verification methodologies
— Comprehensive guidelines for system-level verification
— A complete solution for chip and system verification

Electronic design verification is an inherently risky undertaking. The end product is smaller than a thumb nail yet contains millions of gates that all must function perfectly together. To remain competitive, design teams must keep up with the generational changes in semiconductor process technology. This requires adopting new design and verification methods every two or three years. Of course, incorporating new verification languages, methodologies, and technologies adds risks of their own to your project. The key to success is appropriately managing all of these risks.

The most crucial step to reduce verification risk is automating the verification process. Cadence® provides verification process automation (VPA), from plan to closure, that removes process risks. This upfront planning process enables you to estimate your resource requirements, assign tasks to each engineer, and define the coverage goals and other metrics you will use to measure your progress.

The entire process from verification plan to closure depends on having the right tools to get the job done. This series of Incisive® technical briefs identifies key Cadence products and their technological advantages that make it easy for you to incorporate new languages, methodologies, and technologies into your verification environment while managing the associated adoption risks.

SCALING UP TO FULL-CHIP AND SYSTEM-LEVEL VERIFICATION

Bugs at the unit level often go undetected, leading to costly delays. With today's complex designs, verification specialists need tools and comprehensive methodologies that can scale up to the full chip and system level. This technical brief focuses on the innovative and easy-to-use abstraction technology embedded in the Incisive platform, Specman® Elite testbench automation, and the new plan-to-closure methodology, which enable teams to reach verification closure more efficiently.

Over the past few years, most advanced ASIC/SoC verification teams have moved to an automated approach to unit-level verification, especially in projects where the cost of failure is measured in millions of dollars. Moving from directed testing to coverage-driven, constrained random test generation has dramatically improved the quality of complex logic blocks. But once each block has been exhaustively verified at the unit level, it is still necessary to perform a thorough full-chip or system-level test.

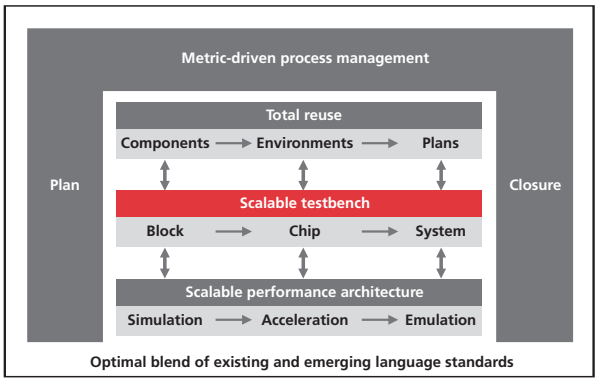


Figure 1: Scalable testbench: block to chip to system-level verification

Today's chips and systems contain numerous IP blocks, on-chip buses, and complex external interfaces that can interact in unpredictable ways to cause problems that are undetectable at the unit level. Checking for bugs exposed by obscure corner cases at the full chip and system level is critical. But many of the same teams that use an automated approach for module-level verification still rely on a hit-or-miss, directed-test methodology with little or no metrics at the full chip or system level. Why? Because the tools and methodologies that work well at the unit level today do not scale up to the chip or system level.

ADDITIONAL REQUIREMENTS

There are a number of additional requirements for managing the added complexity of full-chip and system-level verification.

- Ability to create more intelligent and abstract system-level testbenches that can generate and orchestrate valid stimuli across several interfaces
- Underlying testbench "engines" and analysis tools that scale up to handle huge SoCs

  - Constrained random stimulus generation that can handle tens of thousands of interrelated constraints and schedule sequences across multiple interfaces

  - Coverage engine that can efficiently analyze and merge coverage results for large functional spaces with millions of analysis points

  - Debug facilities for analyzing complex sequences and device under test (DUT) responses, and dealing with hundreds of failures
- Ability to interface a single testbench to different abstractions of the DUT, including SystemC®, transaction level, HDL for RTL, gate level, and acceleration/emulation models
- Ability to reuse multi-language verification IP (Verilog®, VHDL, SystemVerilog, SystemC) at the chip and system levels
- A methodology and pre-defined libraries that link together all of the above, including the reuse of block-level verification components at the chip and system level

After working closely with dozens of customers, Cadence introduced an extended version of Incisive Specman Elite, the system verification methodology (SVM), the *e* reuse methodology (*e*RM), and specialized verification IP building blocks. This is all now included with the Incisive plan-to-closure methodology.

Cadence provides verification process automation, from plan to closure, that removes process risks.

UNIQUE ADVANTAGES OF SYSTEM-LEVEL VERIFICATION TECHNOLOGY

ABSTRACT LAYERED SEQUENCES AND MULTI-CHANNEL STIMULUS GENERATION

Powerful Incisive Specman Elite sequence technology provides a standard means to capture and reuse stimulus sequences from unit to system level, and it enables synchronized stimulus generation from multiple verification components.

Cadence *e* Verification Components (*e*VCs) for the unit level may define sequence libraries that can be easily combined and further constrained at the system level using hierarchical layered sequences. Once these system-level sequences have been established, Specman Elite can then perform multi-channel stimulus generation, which emulates a wide range of complex communications across multiple DUT interfaces.

SUPPORT FOR HETEROGENEOUS VERIFICATION ENVIRONMENTS

As verification environments grow from block to chip to system levels, the use of verification IP (VIP) becomes more prevalent. This may be the result of investment in external VIP or the use of existing internal VIP from a previous project on another project team. It is likely that this VIP may come in multiple languages, prompting the need for mixed-language support.

The new plan-to-closure methodology supports heterogeneous environments. The same multi-channel sequence generation capability that supports *e*VCs can also drive Verilog, VHDL, SystemVerilog, or SystemC BFMs; this enables the verification specialist to leverage the work of design teams and other specialists on the project.

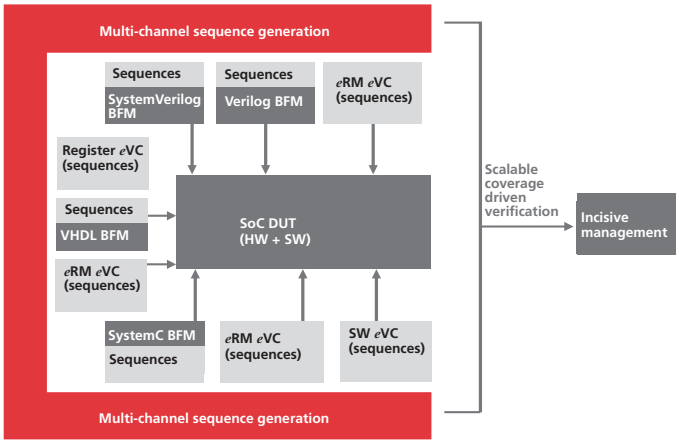


Figure 2: Mixed-language multi-channel sequence generation

Given the sheer number of possible stimulus combinations at the system level, sequences provide the best way to leverage random stimulus generation when creating realistic system-level scenarios. This is in sharp contrast to traditional, "untargeted" data-driven random stimulus tools, which are ineffective at the system level.

As an example, let's take an SoC that has multiple external interfaces, including a gigabit Ethernet port and a USB 2.0 port. One of the target applications for this SoC is the ability to stream MPEG3 audio data from the Ethernet port across an internal bus to the USB port at a specific bandwidth. To verify correct operation, it's possible to generate a set of multi-channel sequences that send MPEG3 data layered on top of an Ethernet protocol stack while also generating the corresponding USB 2.0 device responses.

Specman Elite multi-channel sequence technology enables automatic generation of many permutations of this scenario, including cases that introduce error

Innovative and easy-to-use abstraction technology and the new plan-to-closure methodology enable teams to reach verification closure more efficiently.

conditions. This allows you to thoroughly verify system-level corner cases with minimum effort.

SCALABLE CONSTRAINT SOLVER AND STIMULUS GENERATOR

Verifying large SoCs with realistic system-level stimulus scenarios requires a highly scalable constraint-solver capable of simultaneously resolving thousands of interdependent constraints. Specman Elite's leading-edge multi-channel constraint solver was designed for scalability so that it can efficiently generate the most complex system-level scenarios without creating a bottleneck during system-level simulations.

SCALABLE COVERAGE ENGINE

Given the millions of functional combinations that need to be verified at the system level, the only accurate way to measure and track that all features have been verified is to combine different forms of coverage: functional, code, and assertion. The massive amount of coverage data created throughout the verification of a large system requires a highly scalable coverage engine capable of dumping and merging thousands of coverage files, as well as providing robust analysis to guide verification closure. The Specman Elite coverage engine handles huge coverage data sets while Incisive management provides a rich set of coverage analysis features that allow engineers to leverage the data in a predictable, metric-driven verification process.

SYSTEM-LEVEL DEBUGGING

Specman Elite multi-channel sequence generation combined with its scalable coverage engine help you find more bugs. This necessitates efficient debug capabilities within the verification environment to quickly identify the root cause of each bug. In addition to standard source-level debugging facilities, the Specman Elite visualization toolkit further streamlines the debugging process. This toolkit enables you to create customized visualizations easily, and it provides several built-in tools, including a "stripe chart" transaction-level viewer, register-map viewer, and views of the complete verification environment.

TESTBENCH INTERFACES TO MULTIPLE SYSTEM-LEVEL REPRESENTATIONS

Full-chip and system-level verification takes numerous forms throughout the design cycle-from early architectural validation using SystemC language to late-stage emulation using RTL/structural models and specialized hardware. With Specman Elite technology and the system verification methodology (SVM), the same "golden" testbench can be leveraged across the entire flow, ensuring that each representation of the design is consistent with the previous one.

To facilitate mixed-level verification, Cadence offers a specialized transaction-to-RTL–level port mechanism that bridges SystemC and RTL models. For the extra performance full-chip and system-level verification often requires, Specman Elite with SVM offers testbench partitioning and compilation tools that map the high-activity portions of the testbench into specialized acceleration/emulation hardware for optimum performance.

Only Cadence offers system-level verification that includes the necessary abstractions, engines, and methodologies.

VERIFICATION IP REUSE AND SYSTEM-LEVEL VERIFICATION METHODOLOGIES

Cadence verification methodologies are closely integrated with the underlying technology and are equally important when it comes to addressing the needs of full-chip and system verification. The Incisive plan-to-closure methodology includes not only the system verification methodology, but also the *e* reuse methodology (*e*RM), combining the best practices that enable project teams to ramp-up quickly and efficiently for system-level verification.

*e*RM covers all aspects of building modular verification components for interface protocols, including: generating stimulus sequences, modeling masters and slaves, checking protocol compliance, and measuring functional coverage. *e*RM also ensures that verification components have standard interfaces, so they can be easily reused from unit or block level to subsystem and system-level verification environments, and across multiple projects. *e*RM-compliant components can be easily synchronized and controlled to create complex sequences across multiple interfaces, and thereby stress corner cases.

COMPREHENSIVE GUIDELINES FOR SYSTEM-LEVEL VERIFICATION

As part of the new plan-to-closure methodology, *e*RM is being extended to support SystemVerilog and mixed-language verification environments, and SVM includes a set of comprehensive guidelines and best practices for system-level verification. Specman Elite with the new plan-to-closure methodology (SVM and *e*RM) helps verification teams:

- Use efficient system verification architecture
- Capture and reuse stimulus scenarios, including sequences and multi-channel sequences
- Capture and reuse DUT configurations, including an *e*RM register and memory package for modeling (used to verify DUT behavior under multiple configurations)
- Use a single golden verification environment to connect to all DUT abstraction levels, from SystemC to RTL to acceleration/emulation
- Drive mixed-language verification components with multi-channel sequences for full-system scenarios
- Use a methodology for HW/SW co-verification that verifies combinations of HW/SW with controllability over both parts simultaneously

A COMPLETE SOLUTION FOR CHIP AND SYSTEM VERIFICATION

To avoid the huge costs associated with letting logic errors slip through to silicon, engineers must perform thorough chip and system-level verification. Only Cadence offers a comprehensive and scalable solution for full-chip and system-level verification that includes the necessary abstractions, engines, and methodologies.

FOR MORE INFORMATION

Email us at info@cadence.com or visit www.cadence.com.

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