

# CADENCE AMS METHODOLOGY KIT

The Cadence® AMS Methodology Kit employs the Cadence Advanced Custom Design (ACD) methodology, which leverages silicon-accurate design methods to enable design teams to create differentiated silicon faster and with less risk. The kit delivers verified, packaged methodologies (demonstrated on a real-world mixed-signal design) along with applicability consulting.

## PREDICTABLE, SILICON-ACCURATE RESULTS

The Cadence AMS Methodology Kit executes a “meet in the middle” approach to mixed-signal design that uses a rich suite of methodologies around key design tasks and advanced technologies. This approach combines the best of top-down (behavioral and mixed-level approaches) with bottom-up (transistor-level design and abstraction) design techniques to achieve predictable, silicon-accurate results for complex mixed-signal designs.

Demonstrated on a silicon-implemented and verified Ethernet PHY with 20K analog devices and 30K digital gates, sample simulations, analysis, and physical design approaches, the kit leads a design team through a step-by-step example that shows how to apply Cadence technologies to best achieve design success.

A design team can use the reference design as a basis to understand the methodology, and then map the demonstrated proven techniques and technologies to their own

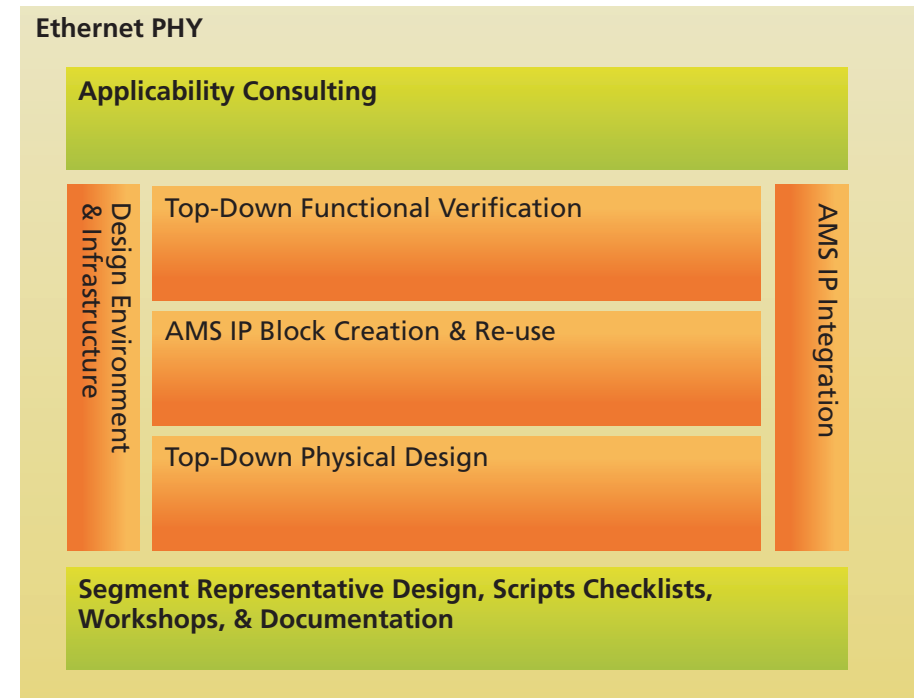


Figure 1: Cadence AMS Methodology Kit and components

designs, thus creating a realizable action plan to improve their own design process. The step-by-step approach allows a team

to absorb and understand a wide array of technologies used to optimize complex analog mixed-signal design processes.

## BASED ON 15 METHODOLOGY MODULES IN A SCENARIO-BASED MODULE APPROACH

Scalable and expandable methodologies that focus on design task execution based on recommended use-model and automation through in-context “scenarios”.

### ANALOG-DRIVEN AMS METHODOLOGY DESIGN FLOW OVERVIEW

- An extensive design and data flow guide from design specification through design manufacturing across different functions of a design team

### ANALOG-DRIVEN AMS DESIGN ENVIRONMENT INFRASTRUCTURE

- Optimal CAD environment setup for design team enablement

### DESIGN PARTITIONING

- Partitioning for ease meet-in-the-middle approach for both functional verification and physical implementation

### DESIGN CONCEPT VALIDATION

- Early behavioral mixed-signal functional verification to mitigate physical implementation risk

### CONSTRAINT-DRIVEN IP CREATE AND RE-USE

- Block IP authoring through physical constraint management

### BLOCK IP YIELD OPTIMIZATION

- Ensure block silicon accuracy through circuit optimization and DFM aware physical optimization

### BLOCK IP CHARACTERIZATION

- Enable block IP re-use through advanced calibrated behavioral modeling

### EXTERNAL BLOCK IP IMPORT

- Ease of IP integration for quick block functional verification and physical assembly

### DESIGN FLOORPLANNING

- Hierarchical mixed-signal chip floorplanning

### DESIGN PERFORMANCE VALIDATION

- Complex mixed-signal functional verification to secure accuracy of physical implementation

### DIGITAL BLOCK AUTHORIZING AND INTER-OPERABILITY

- Digital P&R block authoring for mixed-signal design
- Data and design interoperability between full-custom and P&R design environments

### DESIGN PHYSICAL ASSEMBLY

- Analog constraints driven chip assembly

### DESIGN PHYSICAL VERIFICATION

- Effective chip physical verification and data post-processing for manufacturing readiness

### POST-LAYOUT DESIGN SIGN-OFF FUNCTIONAL VALIDATION

- Post-layout functional verification to ensure chip silicon accuracy for 1st time silicon success

### DESIGN IP PUBLISHING FOR RE-USE

- AMS IP packaging for integration enablement in large SoC design environments

## KIT COMPOSITION AND INTEGRATION

The Cadence AMS Methodology Kit includes the following:

- Complete behavioral models, transistor-level schematics, and layout for the reference design
- Step-by-step documentation
- Advanced custom design methodology, AMS, and physical integration white papers
- Expert applicability consulting designed to map the verified and demonstrated methodologies to a specific customer design

The AMS Methodology Kit relies on and integrates with the following Cadence technologies (not included):

- Virtuoso® Multi-mode Simulation
- Virtuoso Spectre® Circuit Simulator
- Virtuoso AMS Designer Simulator
- Virtuoso UltraSim Full-chip Simulator
- Virtuoso Schematic Editor L, XL, GXL
- Virtuoso Analog Design Environment L, XL, GXL
- Virtuoso Layout System L, XL, GXL
- Virtuoso Layout Migrate
- Virtuoso Analog VoltageStorm® Option
- Virtuoso Analog ElectronStorm Option
- Assura™ Design Rule Checker (DRC)
- Assura Layout vs. Schematic Verifier (LVS)
- Assura Parasitic Extraction (RCX)
- SoC Encounter™ L netlist-to-GDSII configuration for flat designs; part of the Encounter® digital IC design platform

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