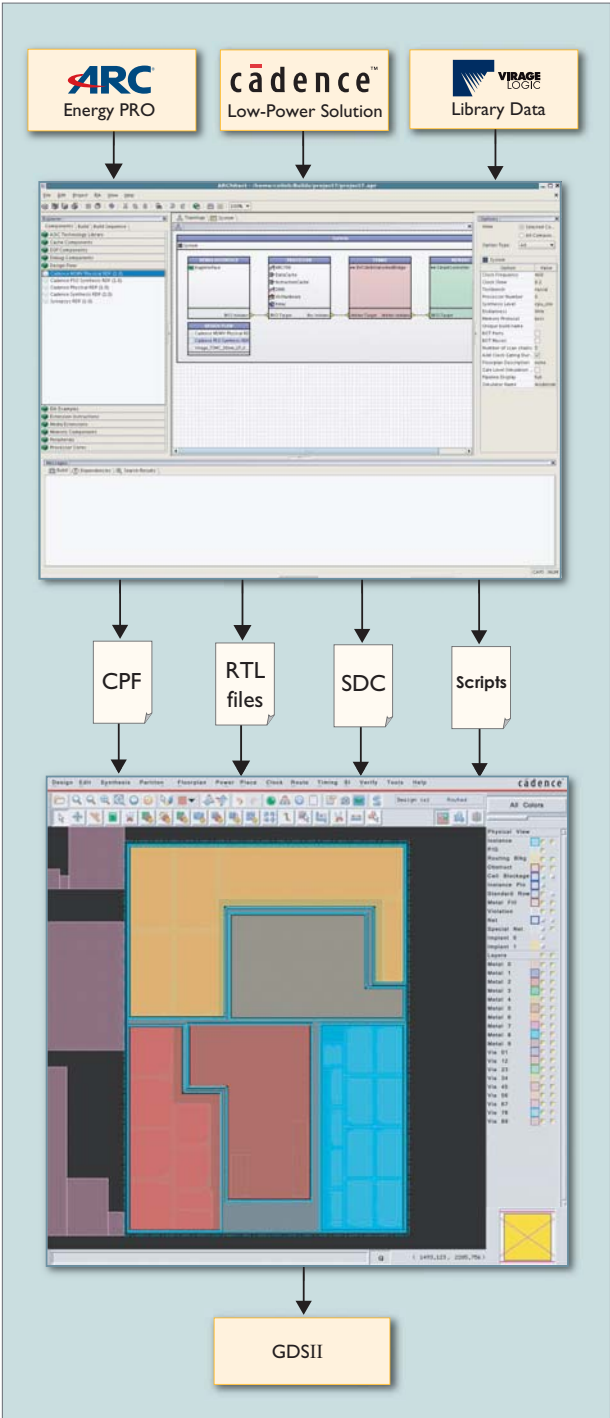


ARC's Energy PRO Technology and Cadence Low-Power Solution Enable Efficient Power Management for Emerging Portable Applications



As chip designs move to 90nm process nodes and beyond, power management becomes a serious concern across the entire design and manufacturing chain. This concern is not limited to battery operated devices – packaging, reliability, and cooling costs make power considerations during design critical for virtually all small-geometry chips.

Advanced power management techniques require an approach to processor design that spans the range of design disciplines and is connected to all design levels. From operating system to layout, chip designers need a holistic approach to ensure maximum power savings. Simple low-power techniques can be applied independently during synthesis and layout; hence we can use mixed Vt cells and implement clock gating, none of which has any great impact on the functionality of the device. However, by themselves, these techniques are no longer sufficient to effectively control a chip's power dissipation.

Advanced techniques actively manage the power profile of the design during its operation and the implementation of these techniques in a new family of ARC® processors has cut across design disciplines, involving operating system design, instruction set, functional design and physical implementation. ARC is adding active power management capability to its future processor cores, comprising a range of techniques including straight-forward clock gating, power shutdown modes, and dynamic voltage and frequency scaling techniques. In addition, ARC and Cadence have partnered to define a low-power design flow that enables ARC designs.

Once the ARC core has been configured, the power intent is captured and written out using Si2's Common Power Format (CPF). This power intent information is then used throughout the implementation flow to ensure that the original power specification has been kept intact from automated synthesis through chip {continued on page 2}

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ARC® Energy PRO & Cadence Low-Power Solution

implementation. ARC® customers can quickly take advantage of the low-power features built into the processor design, using a reference design flow that employs CPF to guide the implementation process and to verify that the initial low-power intent is accurately reflected in the final design.

Energy PRO – Capturing Power Design Intent

Power cannot be considered at a single point in a chip's design; instead, you must consider it throughout the entire flow, from RTL to GDSII, including system architecture, verification, synthesis, physical implementation, Design with Test and formal verification.

ARC is extending its leadership in enabling energy-efficient SoC design by introducing Energy PRO – an integrated hardware/software technology that enables SoC designers to achieve ultra low power operation. Focused on portable applications and combined with existing low-power design techniques, Energy PRO works with ARChitect™, ARC's processor configuration tool, to capture the power design intent of a custom configured ARC processor core. Furthermore, tight coupling with the Cadence™ Encounter® Digital IC Design Platform and low-power logic libraries from ARC partners support a designer's power intent throughout the entire SoC design flow.

Energy PRO includes hardware techniques necessary to conserve energy. At the same time, it includes software components essential for designers to dynamically take advantage of these hardware techniques. Software applications can use the techniques directly using the software APIs and code that ARC provides.

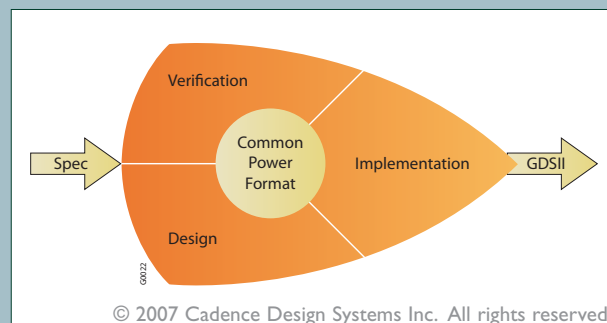
The hardware portion of Energy PRO, which will be integrated in future ARC processor cores, covers ARC and non-ARC IP and provides the logic necessary to generate the correct power management sequences and to control the transition of the hardware between power modes. Energy PRO also provides an interface that SoC designers can use to extend the low-power techniques to other parts of the SoC to implement coordinated power management across the chip, thus deriving maximum benefit from the technology.

There are four key elements of the Energy PRO hardware: Functional Clock Gating, Architectural Clock Gating, Power Shutoff, and Dynamic Voltage and Frequency Scaling.

For Functional Clock Gating (invisible to the user), when a functional block reports that it is idle, Energy PRO turns off the clock to the block to save clock-tree power, reducing power consumption to less than 10% of nominal power consumption. Energy PRO provides multiple power domains, which can be selectively powered-off, bringing the total power consumption to almost zero when the functionality is not needed.

In Architectural Clock Gating, when the processor is in sleep mode and there are no threads or tasks to run, the clocks are gated off to save clock-tree power. Energy PRO's Power Shutoff allows the power supply to the core to be gated off (under software control) when in sleep mode to save leakage power. Finally, Dynamic Voltage and Frequency Scaling reduces the voltage during normal operation when lower performance is acceptable in order minimize the chip's dynamic power {continued on page 3}

Si Common Power Format (CPF) is a file format for specifying power intent early in the design process so that it can be consistently applied throughout the design flow. To save chip power, designers use techniques such as clock gating, multiple threshold voltage libraries, multiple supply voltage (MSV) logic, and power shutoff (PSO), where power is completely turned off for inactive blocks. These techniques require a consistent view in the design steps of logic design, chip implementation, and design verification. As chip design power-awareness has become more pervasive, each EDA tool has independently added the features needed to reflect power intent at that point of the design. Although this makes it possible to build low power flows, power closure is difficult and error prone, since the designer has to specify the same information several times, in several formats, to many different tools. CPF was created as a common format that many tools can use to specify power-specific data, so that power intent only need be entered once and can be used consistently by all tools. The aim of CPF is to support an automated, power-aware design infrastructure, from RTL through GDSII.



A driving force behind the evolution and adoption of CPF is the Power Forward Initiative (PFI), a group of companies that collaborate to drive low-power design methodology and have contributed to the development of the CPF v1.0 specification. PFI membership spans EDA, IP, library, foundries, ASIC, IDM, and other companies. In December of 2006, Cadence contributed CPF to the Silicon Integration Initiative (Si2) where it was ratified by Si2's Low Power Coalition (LPC) as a Si2 standard. The LPC controls the ongoing evolution of the CPF standard. CPF was publicly released in March, 2007.

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dissipation. Dynamically scaling both voltage and frequency when only a subset of functionality is needed can reduce chip power consumption by up to 75%.

ARChitect™ – Custom Processor Configuration

The chip designer configures ARC[®] cores and subsystems using ARChitect, ARC's patented processor configuration tool that enables ARC core users to fully realize the power of ARC's CPU/DSP processors and multimedia subsystems. The ability to custom configure a processor core or subsystem using ARChitect is a fundamental advantage provided to SoC designers of ARC-enabled chips for optimizing power, performance and die size. Configurability allows designers to remove unneeded functionality to reduce die size and power consumption. Furthermore, designers can define custom instructions and IP blocks using the ARChitect Extension Wizard to optimize power consumption.

ARC's future products based on Energy PRO technology will extend this advantage by incorporating specific power management features in the core and then providing design tools which recognize the power intent of the designer and insure that the hardware design provides the optimal energy efficiency.

Using ARChitect's GUI-based development environment and a simple drag-and-drop menu, SoC designers select from 20,000+ pre-configured options and/or create custom instruction extensions that are optimized to the 16-/32-bit ARCompact™ ISA. ARChitect quickly generates a highly differentiated, proprietary ARC-Based™ processor or subsystem that consumes less power and has fewer logic gates than can be created using a "fixed architecture" alternative.

ARChitect configures the chip design together with the design flow and library data. The library data used for flow development, including specialized low-power cells, comes from Virage Logic. CPF describes the power intent and ensures consistent implementation across all tools in the design flow.

Combining Energy PRO with Cadence Encounter Platform

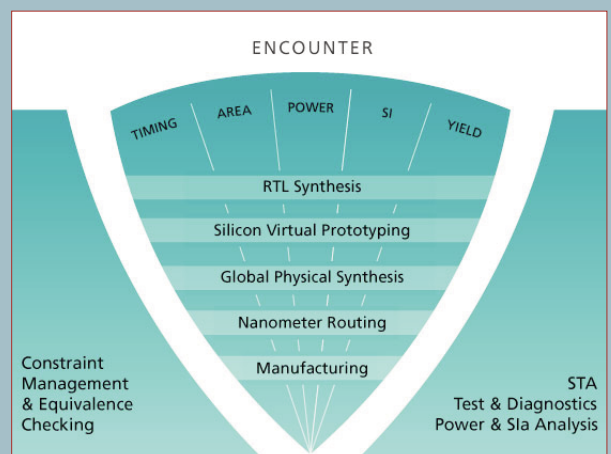
For the most effective implementation of Energy PRO, ARC provides an automated reference design flow created in partnership with Cadence and Virage Logic. ARChitect generates CPF-based specifications to capture the power intent of a custom configured ARC-Based™ chip and to communicate to the Low Power Reference Design Flow (RDF), jointly developed by ARC and Cadence, which tightly integrates the ARChitect Configurator with Cadence Encounter tool chain.

ARChitect allows the designer to configure the Energy PRO-based ARC IP and generate a Cadence Encounter-based

backend flow tailored to the configured ARC IP. To implement various Energy PRO features ARC takes advantage of Virage Logic's Low-Power Standard Cell libraries which provide features to facilitate power management such as isolation cells, level shifters, and others. It is not enough to create low-power technology – low-power intent must be conveyed from the start of the design to tapeout. Energy PRO together with integrated industry-leading EDA tools such as Cadence Encounter platform results in a drop-in solution and reduces product time to market.

cadence™ Encounter digital IC design platform is an integrated RTL-to-GDSII flow for complex and low-power designs at 90nm and below. Encounter is ideal for complex hierarchical designs up to 100 million gates, aggressive low-power designs, yield-aware designs including 65nm and 45nm, and mixed-signal designs. The design platform offers clock-mesh synthesis, design for yield, mixed-signal capabilities, dataflow-driven macro placement and nanometer routing.

As an integrated RTL-to-GDSII design environment, the Encounter platform provides a complete flow-from RTL synthesis and test design, through silicon virtual prototyping, full-chip partitioning and implementation, to final timing and manufacturing closure. Encounter enables high-quality silicon. As an integrated RTL-to-GDSII design environment, the Encounter platform provides a complete flow-from RTL synthesis and test design, through silicon virtual prototyping, full-chip partitioning and implementation, to final timing and manufacturing closure. Encounter enables high-quality silicon design (timing, area, and power with wires), accurate verification, signal-integrity-aware routing, and the latest yield-enhanced and low-power designs.



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ARC® Energy PRO & Cadence Low-Power Solution

ARC International

ARC International is the leading provider of configurable media subsystems and cores. They enable customers to develop SoCs that consume less power, are clone resistant, and are highly differentiated. ARC's configurable products have been adopted by more than 140 companies worldwide that collectively shipped 200 million ARC-Based™ SoCs in 2006. Analysts predict there will be 1 billion SoCs shipping to market incorporating a configurable CPU by 2010. Visit www.arc.com to find out more.



Cadence OpenChoice IP Program

The Cadence OpenChoice IP program enables interoperability and facilitates open collaboration with leading IP providers to build, validate, and deliver accurate models for Cadence design and verification solutions. The program aims to ensure IP quality, integration, and provides engineers access to a broad IP offering through a complete IP catalog. This optimizes the electronics design chain and accelerates customer time to market. For further information contact openchoice@cadence.com.



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