

CADENCE FUNCTIONAL VERIFICATION KIT FOR ARM

To reduce risk, achieve predictable verification closure, and deliver innovative products on time, engineers need automated verification process management, IP reuse, and the latest verification technologies. The Cadence® Functional Verification Kit for ARM offers design and multi-specialist teams a complete solution tailored to ARM® microprocessors that spans the entire verification process. The Kit integrates with the Incisive® verification platform and the proven Incisive Plan-to-Closure Methodology, and is demonstrated on an ARM926™ processor-based design.

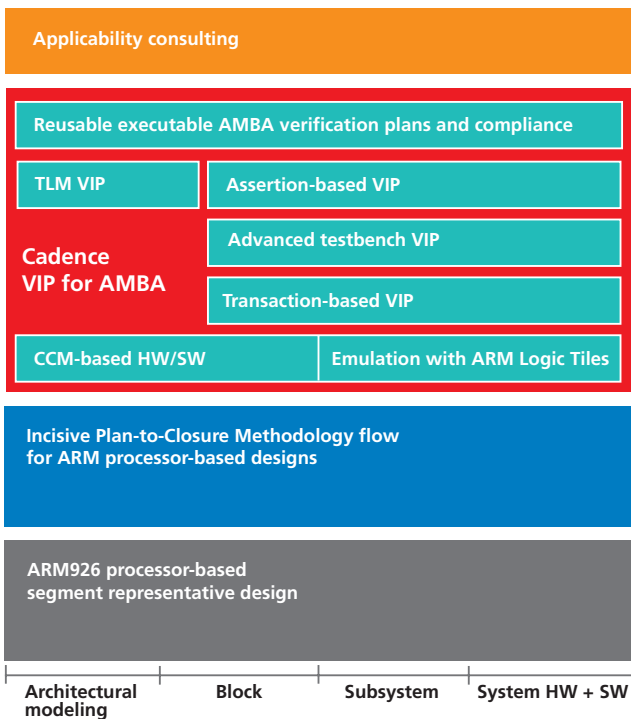


Figure 1: Cadence Functional Verification Kit for ARM

With unforgiving market windows and ever-increasing demand for more functionality and performance packed into single chips, design and verification engineers face a paradox within various market segments such as wireless and consumer. Delivering better products requires incorporating new technologies and, as a result, adds risk to the design and verification process. As these challenges increase, customers need a verification process that is easy to adopt, uses the latest techniques, boosts productivity through automation and IP reuse, and increases predictably to meet their delivery goals.

CADENCE FUNCTIONAL VERIFICATION KIT FOR ARM

Jointly developed by Cadence and ARM, the Cadence Functional Verification Kit for ARM offers a comprehensive verification solution specifically for engineers developing ARM processor-based designs. The Kit contains ARM processor-based verification methodology and flows, a segment representative design, verification process automation (VPA) technology, and reusable verification IP (VIP). The proven Incisive Plan-to-Closure Methodology from Cadence has been tailored specifically to ARM processor-based designs.

Combined with the Incisive platform's VPA technology and ARM processor-based VIP, the Kit verifies both hardware and software from block to chip to system levels. The Kit guides engineers through the following processes and flows to provide a streamlined path from verification plan to closure:

- Advanced verification architecture, maximizing reuse from block to chip to system
- Automated verification planning and management
- Architectural modeling for early HW/SW co-verification
- Assertion-based verification for formal analysis, simulation, acceleration, and emulation
- Testbench automation to address corner-case bugs
- Certified ARM technology-certified AMBA® VIP and protocol compliance
- Transaction-based acceleration for high-performance RTL verification
- In-circuit emulation for system and software validation

The Cadence Functional Verification Kit for ARM demonstrates the verification flows on an ARM926-based segment representative design, which consists of the ARM926 processor, memory subsystem, interrupt controller, DMA, and interface peripherals. The Kit contains documented best practices, "golden" executable examples, and libraries (building blocks and utilities commonly required for SoC design and verification). Also included in the Kit is a comprehensive portfolio of customer-proven VIP that consists of executable compliance verification plans; technology-certified AMBA assertions for formal analysis, simulation, and acceleration; advanced simulation-based testbench components; transaction-based components for simulation and acceleration; and an ARM926 Logic Tile prototype hardware board for in-circuit emulation.

Design and verification teams can use the segment representative design as a basis to understand the recommended methodologies, and then map the demonstrated techniques, technologies, and VIP to their own designs. This provides a proven and realizable plan to improve their verification process. This step-by-step approach allows a team to absorb and understand a wide array of technologies that can optimize the verification solution they need and address the unique challenges they face in verifying ARM processor-based designs.

With expert services and applicability consulting, a prescribed methodology, proven VPA technology, robust VIP, metric-driven verification and management, and representative examples, customers designing ARM processor-based products can increase the predictability of meeting product development milestones, lower adoption risks, and achieve their time-to-market goals.

BENEFITS

- Increases predictability by automating the management of the verification process
- Ensures process management and AMBA specification compliance via an executable verification plan
- Reduces risk by leveraging the industry-proven Incisive Plan-to-Closure Methodology
- Enables VIP reuse across block, chip, and system levels
- Ensures product quality by verifying HW/SW simultaneously at the block, chip, and system levels
- Improves productivity and ease-of-adoption with architectural modeling techniques, formal analysis, simulation, advanced testbench, acceleration, emulation, and HW/SW co-verification
- Based on IEEE standard languages: *e*, SystemVerilog, SystemC®

KIT COMPOSITION AND INTEGRATION

The Cadence Functional Verification Kit for ARM includes the following:

- Prescribed verification methodology from verification plan to closure tailored for ARM processor-based designs
- Full ARM926 processor-based segment representative design and verification environment, including architectural, simulation, RTL, and software views
- Step-by-step documentation and "golden" examples
- Reusable block- and system-level VIP products for verification management, AMBA compliance, formal analysis, advanced testbench, acceleration, and emulation based on years of successful use with hundreds of customers
- Expert consulting designed to map the verified and demonstrated methodologies to a specific customer design

The Cadence Functional Verification Kit for ARM relies on and integrates with the following technologies (not included):

- Incisive Plan-to-Closure Methodology
- Incisive Enterprise Manager
- Incisive Enterprise Specman® Simulator
- Incisive Enterprise Specman Elite®
- Incisive Enterprise Scenario Builder
- Incisive Palladium® series
- Incisive Design Team Manager
- Incisive Design Team Simulator
- Incisive Formal Verifier
- Incisive Xtreme® series

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