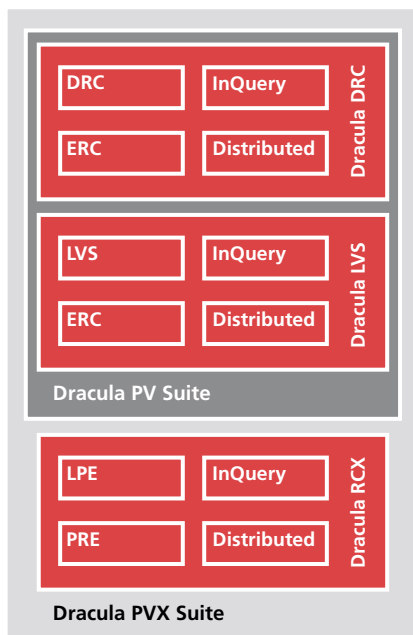


DRACULA VERIFICATION

For more than a decade, IC designers have relied on Dracula® verification to find design errors in their layouts before manufacturing. It is the most widely used final physical verification software in the world. Dracula verification provides comprehensive and accurate verification for all design types—and it’s trusted because it gets the right answers. Software modules perform geometric, electrical, and connectivity checks, as well as parasitic resistance and capacitance extraction.

REPACKAGED DRACULA



Starting with the IC445 release, Dracula has been repackaged to provide better product bundles. These bundles make it easier for you to purchase the tools you require

ADVANCED VERIFICATION FUNCTIONALITY

In addition to basic verification functionality, Dracula provides you with a complete set of verification tools suitable for all designs, from small cells to very large ICs. Dracula supports two modes of operation, flat or 2-level hierarchical verification. Dracula verification handles overlapping cells, geometries that overlap cells from other levels, abutting cells, and over-the-cell routing. It also handles feedthroughs in a layout that may not match the netlist version of a cell. Whether the design methodology is bottom-up, custom, standard-cell, structured gate array, or block-oriented, this technology and its hierarchical processing methods shorten the verification cycle.

DRACULA DRC

Dracula Design Rule Checker (DRC) is an integral component of this physical verification system. It performs checks on layout geometries, gives confidence that the layout can be manufactured, and offers high yields for a given IC process technology.

- A rich set of design rules that support all-angle dimensional checking (spacing, enclosure, width, length, area and overlap)
- Conjunctive rule specifications and a powerful selection capability simplify the incorporation of the most complex IC design rules
- Results from operations can be passed onto subsequent checks for further processing
- Advanced commands support end-of-line via/contact enclosure checking and layer coverage checks

DRACULA ERC

Dracula Electrical Rule Checker (ERC) checks your layout for electrical rule violations such as open circuits, short circuits, and floating nodes. This tool also detects invalid devices and improper implant types, substrate bias, power connections, and ground connections. It eliminates the time-consuming process of finding shorts between global signals by isolating the location at which a short occurs. This checker catches gross electrical mistakes on the layout and gives the designer the confidence that the chip will work the first time.

- Powerful commands to detect electrical rule violations, such as floating devices and improper implants, accelerate the design process by making it easy to find and correct gross violations
- Soft connection capability allows unidirectional passing of nodal information from a connecting layer to a soft connected layer

DRACULA LVS

Dracula Layout versus Schematic (LVS) is used to identify device or network discrepancies between the layout and schematic. Use of this verifier during the IC design process guarantees that the circuit in the mask layout matches the schematic description. It can also be used to identify discrepancies between two similar representations—layout vs. layout (LVL) or schematic vs. schematic (SVS). This tool isolates discrepancies between the two representations of the design and clearly reports the differences for analysis. Using this verifier has resulted in tens of thousands of working semiconductors on the first iteration with considerable savings in processing costs.

- Enables device size comparison of transistors, capacitors, diodes, and resistors within user-specified tolerances and isolates all connectivity problems quickly
- Short circuit identification and isolation features allow rapid location of shorts between labeled nets such as power and ground

- Blackbox capability provides flexibility for handling pre-verified sections of the design or imported blocks
- Accepts a variety of netlist and layout formats, hence eliminating netlist and layout database conversions and minimizing layout vs. schematic preparation time
- Technology independence makes this verifier suitable for all processes, including CMOS, BiCMOS, Bipolar, and GaAs

DRACULA RCX

Parasitic elements have a significant impact on performance in today's high-speed IC designs. With the smaller geometries of leading-edge processes, delays caused by interconnect are becoming increasingly dominant over gate propagation delays. Dracula Parasitic Extraction (RCX) extracts parasitic devices from the integrated circuit layout for input to any circuit simulation. It can dramatically increase the probability of delivering first pass silicon that meets performance criteria.

- 3-D formula-based extraction calculates overlap and fringe capacitance accurately and quickly
- Selected net extraction allows users to scrutinize resistance and capacitance values for critical nets and paths
- Automated rules file generation simplifies the process of developing extraction rule decks
- Technology independence makes layout parameter extractor suitable for all processes, including CMOS, Bipolar, BiCMOS, and GaAs
- Distributed RC network representation of long interconnects for high performance circuits improves the accuracy over lumped RC
- Lumped capacitance extraction capability reduces runtimes
- Outputs RC interconnection information in detailed standard parasitic format (DSPF), which can be used with any delay calculator to produce a standard delay format (SDF) file for simulation

DRACULA GUI OPTION

Dracula Graphical User Interface (GUI), an interactive error debugging and analysis tool, assists in the identification, analysis, and correction of layout errors by displaying the original design layers merged with the system's verification error data in a single window. Debugging and analyzing errors can account for up to 80% of the verification cycle time, but this debugging environment speeds the error correction process by providing online access to verification error information, along with node and device connectivity data.

- Integrates seamlessly with Virtuoso® Layout Editor
 - Automatic step through feature graphically identifies and analyzes DRC and LVS errors from within the Virtuoso environment
- Error analysis and correction takes place in the original Cadence® Design Framework II database when used with Virtuoso Schematic Composer and Virtuoso Layout Editor
- Interactive traversal of circuit netlist allows the display of multiple views of network hierarchy
- Parasitic viewing enables detailed graphical analysis of RC elements in the layout and specific to critical nets
- Graphical cross-probing between netlist, schematic, and layout windows reduces time spent debugging LVS discrepancies
- Interactive short locator rapidly identifies and isolates short circuits in the layout
- Visual access to connectivity, device, and nodal information helps debug layout errors quickly

DRACULA MULTIPROCESSOR OPTION

As today's wafer fab technologies migrate to smaller feature sizes, the circuit transistor counts increases. Verification/design cycle time typically requires overnight results. If results are not available in less than 12 hours, design and layout changes tend to invalidate the verification. Dracula Multiprocessor Option meets this requirement by dividing the verification work over several machines running in parallel, resulting in dramatic reductions in design rules checker run times.

- Divides the verification process between multiple CPUs
- Excellent approach to cutting verification runtimes
- Supports multiprocessor systems and networked distributed processors
- Analyzes rule decks for the most efficient processing of rules
- Only requires two simple additions to the command file

FOR MORE INFORMATION

Email us at icinfo@cadence.com or log on to www.cadence.com

