DATASHEET

EFFECTIVE CURRENT SOURCE MODEL (ECSM)

The Cadence® effective current source model (ECSM) is the industry's first and only production-proven current source modeling standard for timing, power, noise, and variation. This highly accurate open-source model delivers accuracy to within 2% of SPICE and is a critical component of today's advanced low-power and nanometer design flows.

EFFECTIVE CURRENT SOURCE MODEL (ECSM)

Conventional delay modeling formats can differ from SPICE by as much as 20-30%. Non-linear delay models (NLDMs) have reduced accuracy for long nets; they can't add voltage sources to properly model multiple parallel drivers; nor do they accurately account for non-linear IR drop affects on delay. Composite current source models (CCSMs) are unsuitably large and not production-proven.

The Cadence effective current source model (ECSM) is an extension of the Liberty (.lib) timing library format, proven to provide accuracy to within 2% of SPICE in production environments. ECSMs are crucial for today's advanced low-power designs, which require accurate modeling of multiple voltage levels, long interconnects, meshes, and IR drop effects.

ECSMs provide better accuracy for long chip-level interconnects (buses, clocks), parallel drivers (clock meshes), and modeling of voltage impact on delay (IR drop, dynamic voltage scaling). Based on the proven Cadence VoltageStorm® library format and characterization, ECSM power extensions provide actual dynamic current drawn from the power grid for individual cells, and they allow for storage of current waveform at power-grid pins. Based on the proven Cadence CeltIC® cdb models, ECSM signal integrity (SI) extensions provide accurate SI glitch and delay effect modeling. ECSM statistical extensions provide accurate, holistic modeling of process and environmental variation.

With more than 200 tapeouts at 130nm and 90nm in just four years, ECSMs are a truly open standard, approved by the Si2 Open Modeling Coalition and supported by leading companies such as Artisan, TSMC, Virage Logic, and Virtual Silicon.

BENEFITS

- Delivers accuracy to within 2% of SPICE
  - Other common models are only within 20-30% of SPICE
- Ideal for advanced low-power designs
  - Supports advanced low-power techniques (state-retention power gating, dynamic voltage and frequency scaling, multi-supply multi-voltage)
- Provides accurate, holistic modeling of timing, power, noise, and variation
  - Non-linear transistor behavior
  - Receiver pin-cap modeling
  - Time quantized Ceff
  - Voltage impact on delay
- Approved and maintained by Si2 as an open standard
  - Supported by several major library vendors
  - Production-proven delay modeling (200+ tapeouts)

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FEATURES

PRODUCTION-PROVEN DELAY MODELING

- Input slew and output load to determine cell delay
- Time-quantized Ceff
  - C-effective that varies with the output frequency
- I/V curve for each slope, load combination
- Voltage-based measurement for characterization
  - Easily builds on existing voltage measurement and characterization techniques
  - Voltage waveform (V/T) is converted to a current-voltage waveform (I/V) during delay calculation
- Multi-piece pin-cap modeling to accurately model receiver pin-caps

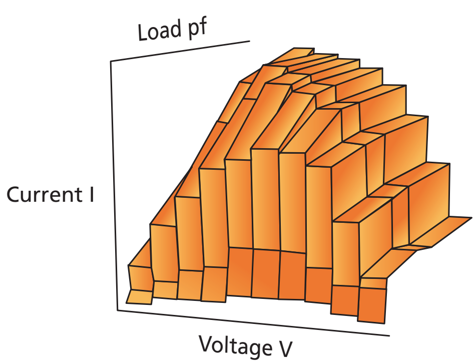

Figure 1: I/V curve for each slope, load combination

RECEIVER PIN-CAP MODELING

- On short RC networks, receiver-pin capacitance dominates net capacitance
- A single receiver pin capacitance value is not accurate since it varies with input waveform
- Accounts for these receiver-pin “miller capacitance effects” using a multi-piece capacitance model that varies as the input transitions
- Accurately captures the waveform-dependent, non-linear behavior of the receiver-pin capacitance

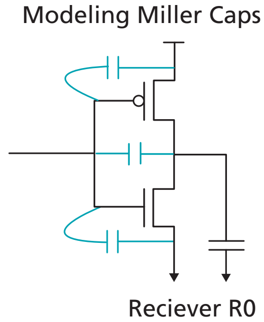

Figure 2: ECSMs accurately capture the waveform-dependent, non-linear behavior of the receiver-pin capacitance

TIME-QUANTIZED CEFF

- Cell delay based on input slope, output load
- RC networks loading modeled as an effective capacitance (Ceff)
  - Ceff is a function of frequency
  - A single Ceff is not accurate for a long RC network
- ECSMs enable time-quantized Ceff, which accurately captures the frequency-dependent effects on delays that are missed with a single Ceff

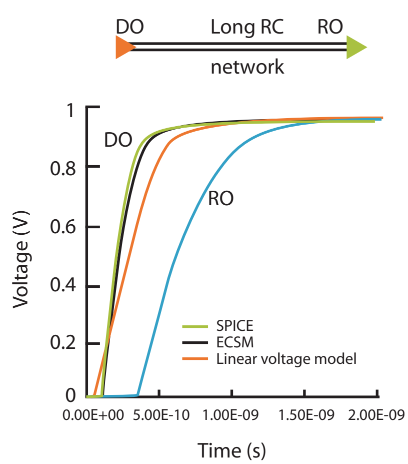

Figure 3: Time-quantized Ceff provides tight correlation with SPICE for long RC networks

VOLTAGE IMPACT ON DELAY

- Libraries only need to be characterized for three voltages
- Delay calculator will employ non-linear interpolation for any cell at any voltage between voltage levels
- Non-linear extrapolation will use outside the characterized range
- Support for state-retention power gating (SRPG), dynamic voltage and frequency scaling (DVFS), and multi-supply multi-voltage (MSMV)

SPECIFICATIONS

LIBRARY VENDOR SUPPORT

- Artisan SAGE-X, SAGE-HS, and Metro standard cell libraries
- TSMC 65nm Reference Flow 6.0
- Virage Logic IPrima Mobile platform
- Virtual Silicon

EDA PRODUCT SUPPORT

- Cadence Encounter® Timing System, First Encounter® silicon virtual prototyping, SoC Encounter™ RTL-to-GDSII system, and CeltIC NDC
- Magma Blastfusion
- Characterization tools
  - Cadence SignalStorm® NDC
  - Magma SiliconSmart SI

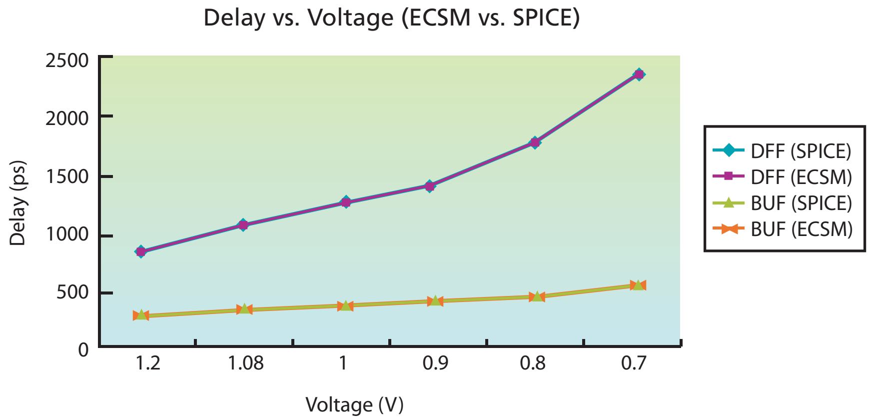

Figure 4: ECSMs show tight correlation with SPICE over varying voltages

FOR MORE INFORMATION

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