

# CADENCE PCB SIGNAL AND POWER INTEGRITY

Cadence provides integrated high-speed design and analysis environment for streamlining the creation of high-speed interconnect on digital printed circuit board (PCB) systems. A range of advanced capabilities make it easy for electrical engineers to explore, optimize, and resolve electrical performance-related issues at all stages of the design cycle. By enabling a constraint-driven design flow this unique environment increases the likelihood of first-time success and reduces the overall costs of end-products.

Cadence PCB signal and power integrity technology is available in the following product offerings:

- Cadence Allegro PCB SI L, XL, and GXL
- Cadence OrCAD Signal Explorer

## CADENCE PCB SIGNAL AND POWER INTEGRITY TECHNOLOGY

Cadence® PCB signal integrity (SI) and power integrity (PI) technologies provide a scalable, cost-effective pre- and post-layout system interconnect design and analysis environment. They deliver advanced analysis at the board, multi-board, and system levels. Cadence PCB SI and PI products integrate tightly with Cadence PCB editors, Cadence Allegro® PCB Router, Allegro Design Entry HDL, and Allegro System Architect, enabling end-to-end, constraint-driven, high-speed PCB system design.

Cadence PCB SI addresses the challenges created as a result of increasing design density, complexity, and faster edge rates by enabling designers to address high-speed issues throughout the design process. This approach allows design teams to eliminate time-consuming simulate-fix-simulate iterations at the back-end of a design process. It also enables designers

to maximize electrical performance while minimizing cost of the overall product by exploring topologies and models with manufacturing tolerances. Cadence PCB SI allows users to weigh the trade-offs involved in routing choices (rules) that affect cost relative to electrical performance and reliability. Once developed, these optimum constraints then drive the physical layout and routing of the PCB. The integrated design and analysis environment eliminates the need to translate design databases to run simulations. Designers can also address shrinking timing margins by considering the effects of package design on the overall performance of the signal from die-to-die. Importantly, the integrated flow allows designers to easily perform pre-and post-layout extraction and verification of complex high-speed PCB systems.

Cadence PCB SI and PI technology is available in the following product offerings:

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- Cadence OrCAD® Signal Explorer

## BENEFITS

- Reduces the time required to design high-speed interconnects and increases the likelihood of first-pass success
- Shortens the time required to develop optimum constraints and enables a constraint-driven PCB design flow
- Improves product performance through solution space exploration
- Reduces unit costs of end products by using the Allegro PCB PI Option XL to design the PCB power delivery system network
- Eliminates the need for physical prototypes for multiple qualifications of Multi-Gigabit per second serial links through advanced simulation techniques
- Shortens design cycle time through faster tradeoffs of MGH signals using S-Parameters and single or coupled analytical via modeling
- Improves product quality, cost, and performance
- Saves time via a virtual prototyping environment that is seamlessly integrated with other Allegro platform design products
- Shortens the time required to design-in advanced devices through the use of Cadence design-in IP portfolios

## FEATURES

### INTEGRATED HIGH-SPEED DESIGN AND ANALYSIS

Allegro PCB SI reads and writes to the Allegro PCB Editor database to avoid possible translation issues and allows for constraints and models to be embedded in the board design file. The integrated design and analysis system is aware of multi-net electrical constructs from front to back. For example, differential pairs and extended nets (nets with a series termination) are recognized, extracted, and simulated as one electrical net. (See Figure 1.)

## SOURCE SYNCHRONOUS, COMMON CLOCK SIGNAL DESIGN

### SIGXPLOERER MODULE

Cadence PCB SI technology contains a module for pre-route topology design and analysis even before a schematic is created (the SigXplorer module). This type of analysis is common at the earliest stages of the design cycle when designers assess the impact of using a new device technology or of increasing bus transfer rate. SigXplorer can be used to build and validate detailed electrical topology models and prove the viability of a new technology—before the detailed design process begins.

SigXplorer is a graphical topology design environment that allows design engineers to prototype critical signals, understand sensitivity, and use “what-if” scenarios to develop optimum constraints. By performing this type of analysis at the earliest stages of the design cycle,

designers can assess the impact of using a new device technology or of increasing edge rates.

Using Cadence PCB SI technology, users can extract a net from Cadence PCB editors that provides an electrical view of a physical topology, including vias and changes in interconnect that affect impedance or velocity. This allows the design engineer to perform “what-if” investigations of electrical behavior without having to edit the PCB design. The engineer can investigate the effects of changing parameter values and develop an acceptable solution without disrupting the PCB design process. This ability is available at any stage of the PCB design process, from schematics, from PCB with placement through to a fully routed board.

### SOLUTION SPACE EXPLORATION

Allegro PCB SI provides the best environment for users who need to develop optimal constraints through solution

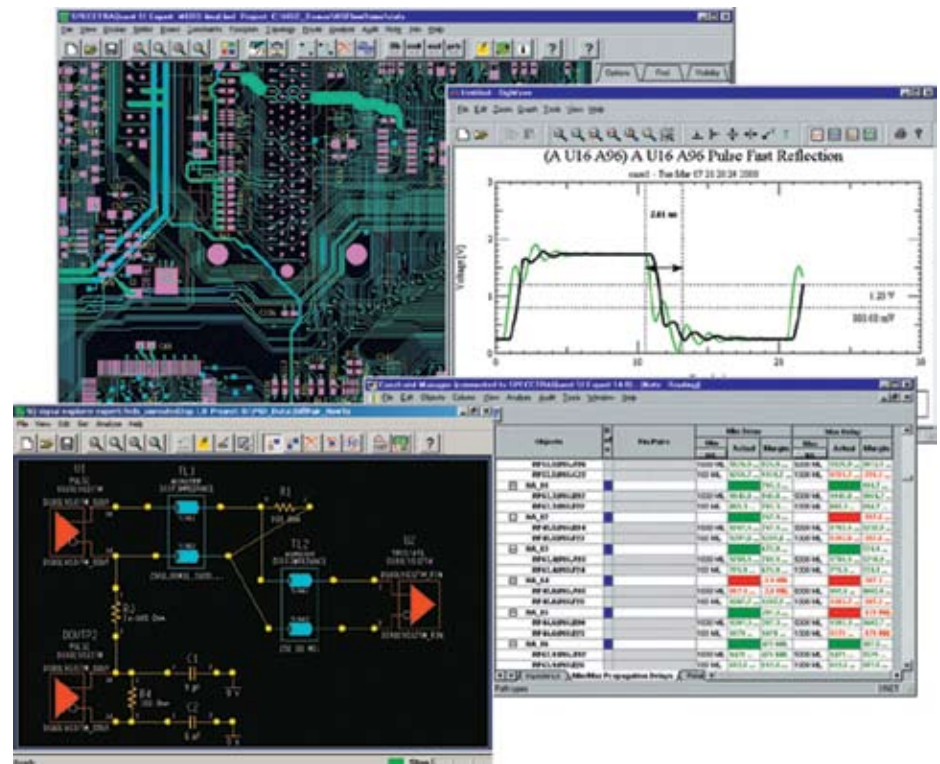


Figure 1: Allegro PCB SI allows engineers to explore and develop optimum constraints with a constraint-driven design flow

space exploration. Solve issues early in the design process by using swept parameter analysis, user-defined stimulus, and custom measurement.

## SPICE-BASED SIMULATOR

Along with a SPICE-based simulator, Allegro PCB SI includes a powerful macro-modeling capability that combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral modeling. An embedded field solver models skin effects, proximity/crowding effects, return path resistance, and frequency-dependent dielectric constant. A robust modeling language provides extensibility beyond IBIS for I/O buffers and lossy coupled frequency-dependent transmission line models that accurately predict the distributed behavior of PCB traces.

## DIE-TO-DIE INTERCONNECT ANALYSIS USING PACKAGE DATABASES

Allegro PCB SI supports multi-board configurations for both analysis and constraints, and provides a simple setup process—from motherboard or daughter card connection to a die-top-die configuration. It also supports topology exploration, floorplanning, and post-route verification.

## INTEGRATED S-PARAMETER SUPPORT

Available as an option to all Cadence PCB SI products, tightly integrated S-Parameter support enables engineers to generate S-Parameters from PCB signal topologies (“Stack-up to S”) and plot in SigWave quickly and easily. Users can change topology or stack-up and do quick iterative loss budget tradeoffs. It also allows designers to concatenate multiple S-Parameters into one, simulate S-Parameters in time domain, and incorporate S-Parameters for an object into the topology and then generate S-Parameters for the entire topology. Additionally, by incorporating S-Parameter support that is flexible, it allows engineers to incorporate measurement-based S-Parameter models in native Touchstone

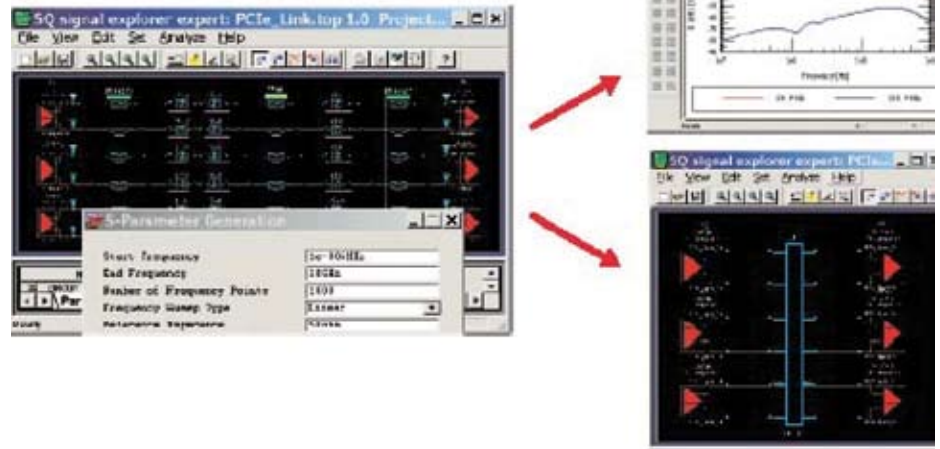


Figure 2: Any portion of the passive interconnect can be plotted as S-Parameter in SigWave topology explorer

format. S-Parameters with other interconnect topologies can also be incorporated, measured, or imported. (See Figure 2.)

## ANALYTICAL VIA MODEL GENERATOR

Users can quickly create accurate via models (wideband, narrowband, S-Parameter) to simulate via stub effects at MGH frequencies for single vias, differential vias, and vias coupled with ground/power vias. Analytical via models can be generated to do via-stub analysis that can dictate either the layers critical signals should be routed or to specify back-drilling of vias on critical nets. Allegro PCB Design XL allows users to specify which vias should be back-drilled during PCB fabrication process.

## BUS ANALYSIS FOR SOURCE SYNCHRONOUS SIGNALS

In the XL and GXL tiers, Allegro PCB SI provides a quick and easy way to do post-layout analysis of all the signals associated with a source synchronous bus. It shortens the time to simulate various configurations (read/write, active, idle) associated with the functioning of source synchronous buses with or without on-die termination (ODT). It allows signals to be associated and to save such associations with the

design database. Users have a choice of doing just reflection analysis or a comprehensive analysis with crosstalk included. Allegro PCB SI provides users a way to derate setup and hold margins through user-defined derating tables for different signals in the source synchronous bus. (See Figure 3.)

## SERIAL LINK DESIGN ENVIRONMENT

Serial link design environment is a virtual prototyping environment for designs with multi-gigabit serial links that shortens design cycle time and eliminates the need for multiple lab qualifications with full functional physical prototypes. This advanced technology offers integrated serial link design and analysis environment built on top of proven Allegro PCB SI capabilities.

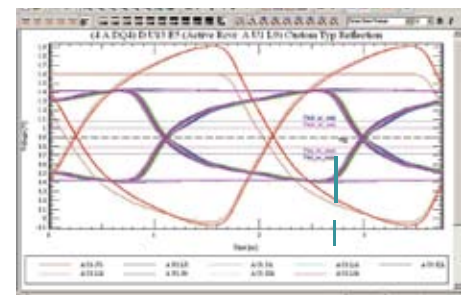


Figure 3: Allegro PCB SI allows engineers to explore and develop optimum constraints with a constraint-driven flow

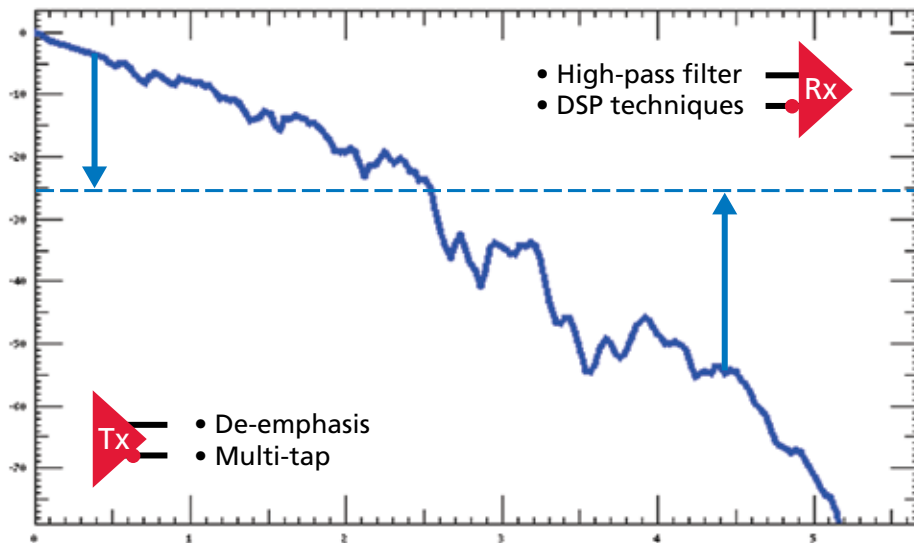


Figure 4: Proven advanced macro-modeling capabilities for devices with pre-emphasis of receiver equalization—without sacrificing simulation performance

Multi-gigabit serial links are driven by transmitters with multi-tap pre-emphasis and receivers with multi-tap equalization. These technological advances allow engineers to architect systems that have higher performance and throughput. However, many of the EDA solutions required to design these systems have not kept pace, leaving engineers forced to use disparate, stand-alone products. Allegro PCB SI GXL addresses the challenges typically created as system designers work to provide ultra-high bandwidth for data transfer against shrinking time-to-market windows.

Another key challenge for multi-gigabit designers is to ensure that the timing and voltage margins are met. As traditional circuit simulators are limited to approximately 1,024 bits of custom stimulus pattern length, the effect of intersymbol interference (ISI) is not adequately modeled. To accurately predict the eye opening, engineers need solutions that can simulate stimulus patterns of 10 to 100 million bits with various noise sources modeled and accounted for.

Designing multi-gigabit serial links requires capabilities that quickly and accurately model each element of the signal's path. This is because at high frequencies the losses on a signal mount as the signal travels through different discontinuities such as vias, connectors,

and different layers in one or more printed circuit boards. Ensuring that losses in critical signals are acceptable is an important step in the design of multi-gigabit serial links. To accomplish this, Allegro PCB SI GXL lets engineers perform loss budget tradeoffs quickly and iteratively using S-Parameters. It also provides a way to change the MGH signal's topology and view expected loss through the system interconnect within seconds. Allegro PCB SI GXL offers engineers an easy-to-use, highly integrated virtual prototyping environment that includes built-in productivity capabilities for MGH designs.

### MACRO MODELING

Macro modeling capabilities enable engineers to model and simulate MGH drivers and receivers faster and more accurately—with simulation performance improvements of 20x to 400x over transistor-level simulation. (See Figure 4.)

### LOSS BUDGET TRADEOFFS THROUGH INTEGRATED S-PARAMETER SUPPORT

Serial link designers can incorporate measurement-based S-Parameter models in native Touchstone format. Combining measured S-Parameter topology elements with designed-in circuit elements allow users to quickly do loss budget trade-offs

with click of a mouse. This integrated S-Parameter support allows users to do quick multiple iterations of what-ifs by changing the topology elements.

### CHANNEL ANALYSIS TO PREDICT BIT ERROR RATE (BER)

Channel analysis provides BER prediction through two approaches. First, it offers BER prediction through time domain bit-by-bit channel simulation. With this approach, users can simulate 10 to 100 million bits in a reasonable amount of time. Second, for channel compliance early in the design process users can use pure statistical analysis method to predict BER.

### CHANNEL SIMULATION

A channel simulation engine within Allegro PCB SI GXL addresses the need for high-capacity, high performance bit-by-bit simulation that can ensure timing and voltage margins are met for MGH signals. This allows users to simulate millions of bits very rapidly. On a typical PC/Windows platform, it can simulate 10,000 bits in just seconds, a million bits in an hour.

Channel simulation is consistent with the traditional circuit simulation methodology. Users can quickly overlay transistor level simulation results on top of channel analysis simulation results. (See Figure 5.)

Systems company users can quickly develop meaningful configurations ("tap settings") for a complex driver or receiver. To determine optimal settings, designers get a recommendation for a specific topology in seconds, saving weeks of simulation time. Users can inject deterministic or random jitter, crosstalk from adjacent channels or signals and data encoding to determine eye height and width.

IC companies can use channel simulation to quickly evaluate if a new device can drive legacy system company channels with frequency offset, Duty Cycle Distortion (DCD) what-if analysis to look at sampling errors and determine how well Clock and Data Recovery (CDR) circuit works in terms of jitter tolerance.

## CHANNEL COMPLIANCE THROUGH STATISTICAL EYE GENERATION

Many systems companies, early in the design process, want to find out if an existing channel can handle higher data rate transmitter and receiver to increase the throughput of the channel. To figure out if a channel can be driven by higher data rate transceivers, Allegro PCB SI GXL provides a statistical eye generation engine. It provides a generic Feed Back Equalizer (FBE), an ideal Feed Forward Equalizer (FFE), and an ideal Decision Feedback Equalizer (DFE). Users can change the number of taps and set the tap coefficients in these built-in models to do channel compliance through a pure statistical analysis. (See Figure 5.)

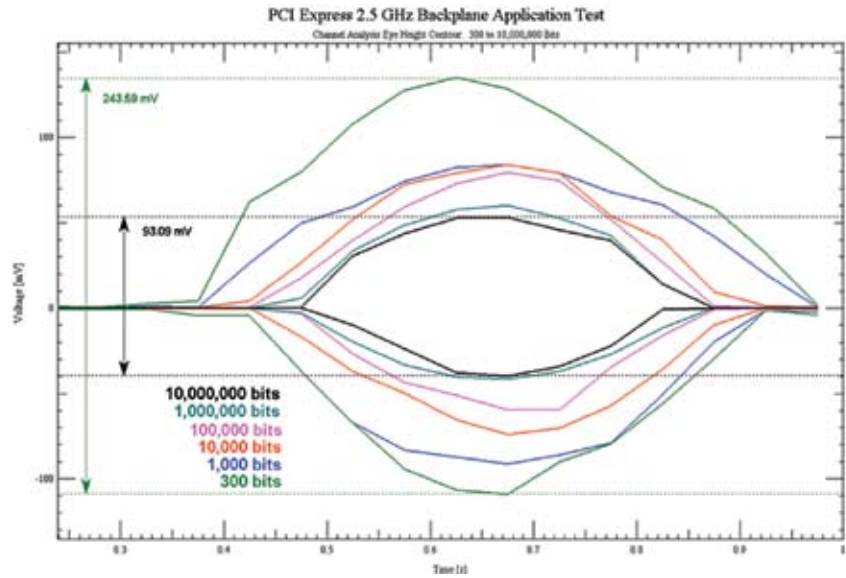


Figure 5: Eye shrinks with number of bits in stimulus pattern. A good eye diagram is important for accurate jitter, insertion loss, and BER prediction

## INTEROPERABILITY OF ADVANCED SERDES MODELS THROUGH ALGORITHMIC MODEL SUPPORT

Devices that operate above 5 Gbps require algorithmic models to model their behavior. Channel analysis allows users to plug-in executable algorithmic models from advanced SERDES IP Vendors. Plug-in executable models are provided in the form of dynamically linked libraries (DLLs).

Channel analysis provides the unique capability of interoperability of advanced SERDES models through the ability to plug-in executable models from IP Vendors.

## CONSTRAINT-DRIVEN PCB DESIGN PROCESS

Cadence PCB SI technology works seamlessly with the constraint management system of Allegro PCB Design Suite.

Constraints derived through simulation can be put into an Electrical Constraint Set (EC Set) from within SigXplorer. These EC Sets can then be applied to other nets in the design through the constraint management system. The constraint management system is found in Allegro PCB SI, Allegro Design Entry HDL and Allegro PCB Design allowing designers to use constraints developed through simulation and exploration and enable a constraint-driven physical layout process. (See Figure 6.)

## ESTIMATED CROSSTALK TABLES

Estimated crosstalk tables generated from Allegro PCB SI enable shorter design cycles and higher densities on the PCB design, possibly reducing end product cost through reduction of layers needed. It allows users to create estimated crosstalk tables to drive interactive and automatic routing to avoid crosstalk issues on the board. Estimated crosstalk tables are generated for each unique driver, spacing, layer-to-layer combination, and simulation mode (fast, typical, or slow). With estimated crosstalk tables and a constraint driven-PCB layout methodology, users can shorten their design cycle time by avoiding crosstalk issues.

## POST-LAYOUT DESIGN VERIFICATION

Allegro PCB SI is seamlessly integrated with Cadence PCB editors. It allows users to do post-layout verification right from the PCB editor. It also allows users to debug critical signals by extracting directly from Allegro PCB design database without any translation. Users can simulate a net, a group of nets or all nets on the board. Model assignment, models, as well as all the simulation-derived constraints are embedded into the PCB design database.

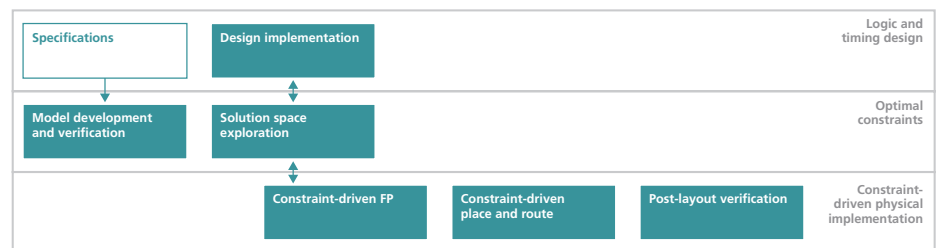


Figure 6: Allegro PCB SI allows engineers to explore and develop optimum constraints with a constraint-driven design flow

## RULES CHECKING USING EMCONTROL

By applying a combination of standard rules and user-defined rules, EMControl can eliminate weeks of manual checking and improve product quality and reliability. For a standard rule set, EMControl provides comprehensive, knowledge-based, design rule checking (DRC) for common EMI-related placement and routing issues. For user-defined rules, EMControl allows creation of custom rules that fit within a company's design guidelines. Importantly, these rules capture the high-speed design "experience" as customized rules, which in turn can be reused on future designs. The EMControl module predicts farfield differential-mode radiated emissions in both SigXplorer and the Allegro PCB SI floorplanner. It also allows for exploration of design strategies required to keep radiation within acceptable levels. Near-field EMI analysis, available within the Allegro PCB SI floorplanner, can predict radiated energy immediately above the board surface. By analyzing near-field EMI patterns, designers can identify which portions of a routed trace are producing the most radiated energy and adapt the design accordingly.

## PCB DESIGN PLANNER

Allegro PCB Design Planner is an option that allows users to develop effective constraints for nets as well as components. Engineers can access thermal analysis, SI, and PI tools to derive constraints on nets and components. When used in conjunction with design creation tools, it allows engineers to specify design intent with constraints embedded in the front end design database.

The PCB design planner option also includes a floorplanning capability that provides a graphical view of the PCB database allowing users to view and edit the PCB design. Designers can quickly and easily evaluate the effects of different placement strategies on design behavior.

## MODEL DEVELOPMENT AND VERIFICATION

Cadence PCB SI technology includes a model integrity module that allows designers to create, manipulate, and validate models quickly in an easy-to-use editing environment. Device model formats supported include:

- IBIS 4.2 External Model support for Verilog®-A, Cadence Spectre®, HSPICE, Cadence eSpice models
- IBIS ICM package and connector models
- Mentor/Quad XTK
- Cadence Device Modeling Language (DML)
- Synopsys HSPICE transistor-level models (requires HSPICE simulator and license, which is not included with Allegro PCB SI)
- Spectre transistor-level models (available on Sun Solaris, HP-UX, and Linux RHEL 3.0 platforms only). This utilizes an integrated and limited capability version of the Spectre simulator, which is included with Allegro PCB SI XL

A Spectre-to-DML conversion module assists in creating DML models from Spectre simulation runs. With the output of the Spectre simulation run, buffer options file, users can quickly create DML models. Model integrity identifies V-I and V-T tables for typical, maximum, and minimum corner cases from the Spectre run file. A proven, intelligent best-curve-fitting algorithm provides an accurate DML model. An HSPICE-to-IBIS conversion module allows users to create IBIS models from HSPICE simulation runs.

## POWER DELIVERY SYSTEM DESIGN

Allegro PCB PI is an option that can be added on to Allegro PCB SI. This unique, integrated design and analysis environment takes the guesswork out of quantifying and controlling noise in power delivery systems. It allows users to focus on the design instead of struggling with

data translation issues between the CAD system and the analysis engines. It integrates proven technology from Sun Microsystems into the Cadence design and analysis environment to address the power delivery issues encountered in high-speed design.

The PCB PI option embodies a methodology used to design and optimize frequency-dependent characteristics (supply path impedance) of power distribution systems in high-speed PCB design. It allows users to do quick and easy iterations of "change-simulate-analyze." The Cadence approach is rooted in the fact that a power distribution system's impedance is frequency dependent and must be analyzed and controlled over frequency ranges of interest. The maximum supply current and the tolerated voltage ripple are used to derive the main power delivery system's design parameter—the target impedance. Optimizing the target impedance over the frequency range in which the system is expected to operate yields a power delivery system without hot spots.

The option offers a unique approach to the actual designing of power distribution systems. It takes the integrated approach a step further by making the debugging of a problem as simple as "click and view." Clicking on a waveform in the waveform display window highlights the corresponding region on the PCB and offers a suggestion on the type and number of capacitors needed to address the problem. Results are displayed in the waveform window. By having a PCB design editor integrated with this analysis environment, engineers can select and place decoupling capacitors in the necessary areas, and then quickly see the problem resolved.

## SETUP WIZARD

Gathers all the necessary pieces for design and analysis including board outline; layer stack-up; power plane shapes/power and ground plane pairs; DC nets associated with the power planes; and capacitor libraries.

## FREQUENCY DOMAIN ANALYSIS

Combines the right frequency domain analysis engine with the proven, powerful Allegro PCB SI and Allegro PCB Design environments. It simulates the problem in the frequency domain to quantify the impedance of the power delivery system across the frequency range of interest. During simulation, it takes into account the entire power delivery system—VRM, bulk capacitors, bypass capacitors, and power planes. It calculates the number and values of decoupling capacitors and guides users in placing them for optimal results. Users can perform single node analysis early in the design cycle to see if the number of capacitors selected can maintain the target impedance over a desired frequency range. And, as capacitors are placed on the board, multi-node simulation, which takes into account the location of the capacitors on the board and the mounted loop inductance, can be easily run.

## VOLTAGE RIPPLES IN TIME DOMAIN

Effectiveness of decoupling capacitor selection and placement can be verified in time domain.

## VRM EDITING

An easy-to-use input inductance calculator and a target impedance calculator make it simple to specify the allowed voltage ripple and dynamic current to compute the target impedance, and the target impedance is shown in the simulation results waveform window. The simulation waveform window displays a target impedance line, which makes it easy to know which regions of the PCB are crossing the target.

## IC DIE AND PACKAGE CHARACTERISTICS

PCB PI option allows users to develop a realistic target impedance by including IC/package inductance, and to assign package and die power delivery models to an arbitrary position on a two-dimensional plane structure on the board to perform multi-node simulations. Users can provide

IC switching current profile, on-die capacitance, IC/package sub-circuit for components on the board. Users also have an option to provide IC/package inductance if a sub-circuit for any of the components is not available. IC switching current profile can be obtained from IC companies. A two-port or a multi-port model of a DC net of an IC/package can be generated from IC/package design and analysis tools.

## STATIC IR DROP ANALYSIS

Users can quickly ensure power distribution system can provide sufficient current to drive signals on the design through Static IR drop analysis. Static IR drop analysis takes into account the trace neck-down, swiss cheese effect created by components with dense pin grid arrays (BGAs) as well reduction of available copper caused by trace routing on power and ground planes. It will also take into account vias that connect multiple ground planes of the same net.

Static IR drop analysis allows users to view results in a graphical voltage drop display or view a report that shows voltage drop at any pin that is marked as a current sink. Users can also view relative and absolute voltage drop at any point on the net.

## COMPLETE DESIGN AND ANALYSIS ENVIRONMENT

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## DESIGN-IN IP PORTFOLIOS

Time to volume production for IC manufacturers depends on quick adoption of new devices by systems companies. However, the combination of differing design environments, complex I/O structures, and multi-gigabit-speed data rates make new device simulation and implementation into a PCB system a complex and expensive process.

Innovative silicon design-in IP portfolios from Cadence and key industry partners tackle these issues. Using technology available in the Allegro PCB SI design and analysis environment, IC manufacturers can help shorten their customers’ design-in time on complex silicon devices by providing an executable version of their design guides in the form of high-speed silicon design-in IP portfolios. These silicon design-in IP portfolios contain ready-to-simulate topologies with pre-validated models, layout constraints embedded in a sample PCB file to enable constraint-driven layout flows, tutorials, documentation, scripts, and other utilities. Design-in IP portfolios allow engineers to accurately simulate PCB topologies with minimal setup, enabling them to obtain accurate simulation results 20 times faster than would have been possible without silicon design-in IP.

All design-in IP portfolios are available for Cadence users to download from [http://www.cadence.com/products/si\\_pk\\_bd/ic\\_design\\_in\\_dt.aspx](http://www.cadence.com/products/si_pk_bd/ic_design_in_dt.aspx)

## DDR2 DESIGN CHAIN

A methodology for designing system-level DDR2 memory interfaces leverages IP from Altera, Micron Technology, and Cadence. The methodology shown in the DDR2 Design-in IP Portfolio can be applied to other high-speed source synchronous signals as well.

## PCI EXPRESS DESIGN CHAIN

As MGH serial interfaces become more common, many systems companies are choosing to use the next-generation PCI bus—PCI Express. The PCI Express design

chain provides an environment in which silicon vendors can communicate the design-in requirements for their devices using PCI Express. Systems companies are able to make trade-offs regarding the performance of member companies' silicon with respect to system requirements.

### CHIP SETS SPECIFIC DESIGN-IN IP PORTFOLIOS

- INTEL IXP2800 NETWORK PROCESSOR DESIGN-IN IP PORTFOLIO

For more information, contact your Intel representative and ask for the hardware design kit (HDK) for the IXP2800 network processor.

- XILINX VIRTEX II-PRO DESIGN-IN IP PORTFOLIO

For more information, visit [www.xilinx.com](http://www.xilinx.com) or contact your Xilinx or Cadence representative.

### MENTOR BOARD STATION FLOW

Allegro PCB SI can be used in conjunction with the Mentor Board Station PCB design system to provide high-speed design and analysis within a Mentor-based PCB design environment. Allegro PCB SI is used to perform high-speed analysis and to define the high-speed design rules used to drive the Allegro PCB Router. Once the design has been placed and routed in accordance with the high-speed rules, the results are passed back to the Mentor Board Station environment. This allows Allegro PCB SI and the Allegro PCB Router to be used for high-speed design and analysis, while the existing Board Station-based manufacturing output process is used for committing the design to manufacturing.

### OPERATING SYSTEM SUPPORT

#### *Allegro platform technology:*

- Sun Solaris
- Linux
- IBM AIX
- Windows

#### *OrCAD technology:*

- Windows

### CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

## MAJOR FEATURE SUMMARY FOR ALLEGRO PCB SI PRODUCTS

| PCB SI product comparison grid (OrCAD, Allegro L/XL/GXL)               | OrCAD Signal Explorer | Allegro PCB SI L | Allegro PCB SI XL | Allegro PCB SI GXL |
|------------------------------------------------------------------------|-----------------------|------------------|-------------------|--------------------|
| Macro modeling support (DML)                                           | •                     | •                | •                 | •                  |
| IBIS 4.2 support                                                       | •                     | •                | •                 | •                  |
| IBIS ICM model support                                                 | •                     | •                | •                 | •                  |
| Spectre-to-DML                                                         | •                     | •                | •                 | •                  |
| HSPICE-to-IBIS                                                         | •                     | •                | •                 | •                  |
| Graphical topology editor                                              | •                     | •                | •                 | •                  |
| Lossy transmission lines                                               | •                     | •                | •                 | •                  |
| Coupled (3 net) simulation                                             | •                     | •                | •                 | •                  |
| Differential pair exploration and simulation                           | •                     | •                | •                 | •                  |
| Custom stimulus                                                        |                       | •                | •                 | •                  |
| Topology append                                                        |                       | •                | •                 | •                  |
| Generate estimated crosstalk tables                                    |                       | •                | •                 | •                  |
| Detailed simulation reports                                            |                       | •                | •                 | •                  |
| Coupled (>3nets) simulation                                            |                       | •                | •                 | •                  |
| Allegro Physical Viewer Plus                                           |                       | •                | •                 | •                  |
| Differential pair extraction from Allegro PCB Editor                   |                       | •                | •                 | •                  |
| Differential pair extraction from Allegro Design Entry HDL             |                       | •                | •                 | •                  |
| Current probes                                                         |                       | •                | •                 | •                  |
| Multi-terminal black boxes in topologies                               |                       | •                | •                 | •                  |
| Custom measurement                                                     |                       | •                | •                 | •                  |
| Post-layout selection and crosstalk simulation from Allegro PCB Editor |                       | •                | •                 | •                  |
| HSPICE interface                                                       |                       | SI Performance   | •                 | •                  |
| Differential signal constraint capture                                 |                       | SI Performance   | •                 | •                  |
| Comprehensive simulation                                               |                       | SI Performance   | •                 | •                  |
| Sweep simulations                                                      |                       | SI Performance   | •                 | •                  |
| Constraint development and capture of topologies                       |                       | SI Performance   | •                 | •                  |
| Wide band analytical via model generator                               |                       | SI Performance   | •                 | •                  |
| Topology apply                                                         |                       | Design Planner   | •                 | •                  |
| Constraint-driven floorplanning and placement                          |                       | Design Planner   | •                 | •                  |
| Allegro Constraint Manager                                             |                       | Design Planner   | •                 | •                  |
| Color-coded real-time feedback on violations                           |                       | Design Planner   | •                 | •                  |
| Spectre transistor-level model support                                 |                       |                  | •                 | •                  |
| Source synchronous bus analysis                                        |                       |                  | •                 | •                  |
| Batch simulation                                                       |                       |                  | •                 | •                  |
| EM Control: rules development                                          |                       |                  | •                 | •                  |
| EM Control: rules checking                                             |                       |                  | •                 | •                  |
| EMI differential simulation                                            |                       |                  | •                 | •                  |
| Constraint-driven routing                                              |                       |                  | •                 | •                  |
| Allegro PCB Router XL                                                  |                       |                  | •                 | •                  |
| Static IR drop analysis                                                |                       |                  | •                 | •                  |
| Simultaneous switching noise (SSN) analysis                            |                       |                  | •                 | •                  |
| S-Parameter DC extrapolation                                           |                       | S-Parameters     | S-Parameters      | •                  |
| S-Parameter generation from stack-up                                   |                       | S-Parameters     | S-Parameters      | •                  |
| S-Parameter plotting in SigWave                                        |                       | S-Parameters     | S-Parameters      | •                  |
| Time domain simulation of S-Parameters                                 |                       | S-Parameters     | S-Parameters      | •                  |
| Library management of S-Parameters in model integrity                  |                       | S-Parameters     | S-Parameters      | •                  |

## MAJOR FEATURE SUMMARY FOR ALLEGRO PCB SI PRODUCTS

|                                                          | OrCAD Signal Explorer | Allegro PCB SI L | Allegro PCB SI XL | Allegro PCB SI GXL |
|----------------------------------------------------------|-----------------------|------------------|-------------------|--------------------|
| PCB SI product comparison grid (OrCAD, Allegro L/XL/GXL) |                       |                  |                   |                    |
| Coupled via model generator for pre-layout explorations  |                       | S-Parameters     | S-Parameters      | •                  |
| High-capacity channel simulation                         |                       | Serial Link      | Serial Link       | •                  |
| Optimum pre-emphasis bit configurations ("tap settings") |                       | Serial Link      | Serial Link       | •                  |
| BER prediction                                           |                       | Serial Link      | Serial Link       | •                  |
| Bathtub curves                                           |                       | Serial Link      | Serial Link       | •                  |
| Channel compliance—statistical analysis                  |                       | Serial Link      | Serial Link       | •                  |
| Post-layout MGH extraction                               |                       |                  |                   | •                  |
| Voltage ripples in time domain                           |                       | PI Option        | PI Option         | PI Option          |
| Impedance requirements calculator                        |                       | PI Option        | PI Option         | PI Option          |
| Decoupling capacitor selection and placement             |                       | PI Option        | PI Option         | PI Option          |
| VRM editor                                               |                       | PI Option        | PI Option         | PI Option          |
| Decoupling capacitor library editor                      |                       | PI Option        | PI Option         | PI Option          |
| Cross-probing between waveform and design canvas         |                       | PI Option        | PI Option         | PI Option          |
| Frequency domain analysis                                |                       | PI Option        | PI Option         | PI Option          |
| IC switching currents                                    |                       | PI Option        | PI Option         | PI Option          |
| Package and die parasitics                               |                       | PI Option        | PI Option         | PI Option          |

### Notes:

SI Performance: Allegro PCB SI Performance Option

S-Parameters: Allegro PCB SI S-Parameters Option

Serial Link: Allegro PCB SI Serial Link Option

PI Option: Allegro PCB PI Option

Design Planner: Allegro PCB Design Planner Option

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