DATASHEET

CADENCE SiP DIGITAL DESIGN

System-in-package (SiP) implementation poses new hurdles for system architects and designers. Conventional EDA solutions have failed to automate the design processes required for efficient SiP development. By enabling and integrating design concept exploration, capture, construction, optimization, and validation of complex multi-chip and discrete substrate assemblies on printed circuit boards (PCBs), the Cadence SiP design technology streamlines the integration of multiple high-pin-count chips onto a single substrate.

Cadence technology for digital SiP design includes three focused products for full SiP implementation:

- Cadence SiP Digital Architect XL and GXL
- Cadence SiP Digital Layout GXL
- Cadence SiP Digital SI XL

CADENCE SIP DIGITAL CO-DESIGN TECHNOLOGY

Manufacturers of high-performance consumer electronics are turning to SiP design because it can provide a number of significant advantages such as increased functional density, integration of disparate chip technologies, low power, improved signal performance/integrity and ease of integration into PCB system. However, this also means it requires expert engineering talent in widely divergent fields, which, to date, has limited mainstream adoption. By streamlining the integration of multiple high-pin-count chips onto a single substrate through a concurrent connectivity driven co-design methodology, the Cadence SiP digital co-design technology allows companies to adopt what were once expert engineering SiP design capabilities for mainstream product development.

Cadence SiP solutions seamlessly integrate into Cadence Encounter® technology for die abstract co-design, Cadence Virtuoso® technology for RF module design, and Cadence Allegro® technology for package/board co-design. (*See Figure 1.*)

A COMPLETE CONNECTIVITY DRIVEN CO-DESIGN SOLUTION

The Cadence digital-driven SiP flow focuses on the design challenges of integrating multiple large high-pin-count chips onto a single substrate. This flow targets the major challenges of SiP level connectivity definition and management, physical concept prototyping of the SiP floorplan, including multi-chip die stacks, and die I/O planning to optimize and minimize substrate connectivity routing and signal integrity challenges. This flow is driven by Encounter and Verilog® connectivity.

cādence™

Cadence technology for digital SiP design includes three focused products for full SiP implementation:

- Cadence SiP Digital Architect for front-end design concept definition and evaluation
- Cadence SiP Digital SI for detailed interconnect extraction, modeling and signal integrity/power delivery analysis
- Cadence SiP Digital Layout for constraint and rules driven detailed physical substrate construction and manufacturing preparation

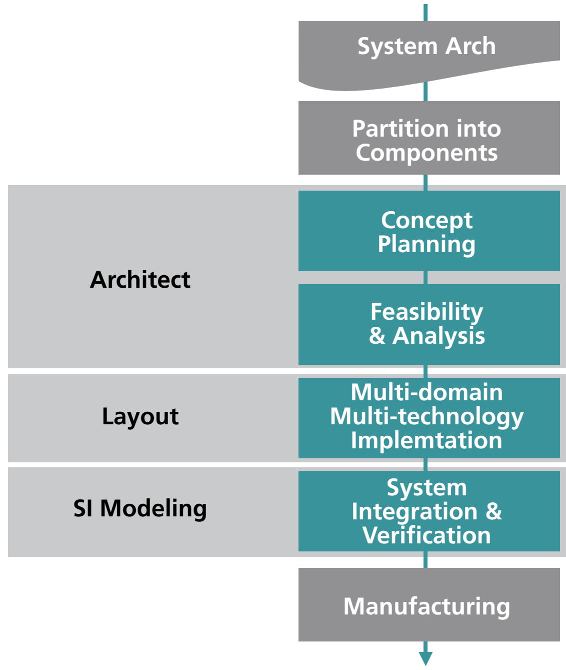

Figure 1: Cadence SiP Digital Co-Design Technology

CADENCE SiP DIGITAL ARCHITECT

Cadence SiP Digital Architect provides a SiP concept prototyping environment for early design exploration, evaluation and tradeoff using a connectivity authoring and driven co-design methodology across die abstract, package substrate and PCB system. Built around a unique System Connectivity Manager, SiP Digital Architect provides the architect with a unique environment to explore and define system connectivity/functionality that is optimized between ICs, SiP package substrate, and target PCB system through concurrent co-design. It allows engineers to perform rapid "what-if" feasibility studies to ensure maximum device functional density performance, while minimizing power consumption. It fully supports IC-driven or package/board substrate-driven flows with cross-fabric domain engineering change orders (ECO) and layout versus schematic (LVS) validation. Since its design focus is predominantly digitally based, analog and/or RF mixed-signal design content is imported and managed as a hierarchical sub-block(s).

BENEFITS

- Allows rapid "what-if" feasibility studies for maximum device functional density, performance, and minimal power consumption
- Enables rapid system-level connectivity capture with ability to bind into alternative physical implementation scenarios to evaluate performance and tradeoffs
- Provides IC I/O padring/array co-design and optimization at the IC, substrate, and system levels

CADENCE SiP DIGITAL LAYOUT

Cadence SiP Digital Layout provides a constraint- and rules-driven layout environment for SiP design. This includes substrate place and route, final connectivity optimization at the IC, substrate, and system levels, manufacturing preparation, full design validation, and tapeout. The environment features integrated IC/package I/O planning capabilities and three dimensional (3D) die stack creation and editing capabilities. In addition, full online design-rule checking (DRC) supports the complex and unique requirements of all combinations of laminate, ceramic, and deposited substrate technologies. Multi-layer flip-chip along with radial any-angle routing substrate routing provide rapid constraint-driven interconnect creation.

BENEFITS

- Provides 3D die stack creation/editing for rapid stack assembly and optimization
- Enables IC I/O pad ring/array co-design and connectivity optimization at the IC, substrate, and system levels
- Allows connectivity assignment and optimization between ICs and substrate for optimized/minimal layer usage based on signal integrity and routability
- Reduces tedious, time-consuming, and manual breakout editing via flip-chip die autoroute-breakout
- Includes comprehensive substrate DFM capabilities for rapid design manufacturing preparation
- Provides 3D design viewer and DRC for accurate full 3D wire bondshell verification, design review debug, and design documentation for assembly and test

CADENCE SiP DIGITAL SI

Cadence SiP Digital SI provides an environment for the co-simulation of SiP interconnect, including embedded ICs and the target PCB. By using its integrated signal integrity, parasitic extraction, and 3D modeling, engineers can make tradeoffs to minimize cost while maximizing performance of the package module interconnect. To model and simulate complex 3D SiP structures, SiP Digital SI includes an embedded 3D field solver, integrated S-Parameter support, and fast, high-capacity simulation (10,000 bits in seconds) to provide a unique combination of fast and accurate multi-gigahertz interconnect analysis.

BENEFITS

- Provides a highly integrated physical and electrical design environment
- Pre-post route interconnect analysis with graphical topology exploration enables rapid what-if performance tuning
- Includes an industry-proven embedded 3D field solver and SPICE-based simulation engine
- Enables rapid evaluation of cost versus performance tradeoffs through its virtual prototyping environment
- Reads/writes Cadence Digital SiP Layout files

KEY FEATURES*

*Reference the product capabilities grid at the end of this datasheet to see what features are applicable to what product.

SYSTEM CONNECTIVITY MANAGER

The System Connectivity Manager is the "cockpit" or "dashboard" of the SiP Digital Architect. It allows the project architect to rapidly author and/or capture the connectivity of the SiP, which includes importing IC die Verilog netlists for chips that comprise the SiP design and interfacing to the PCB footprint symbol of the completed SiP. Embedded LVS routines and ECO management capabilities ensure that the logical SiP definition matches the physical SiP implementation, including any ICs that are partitioned and co-designed as part of the SiP. (*See Figure 2.*)

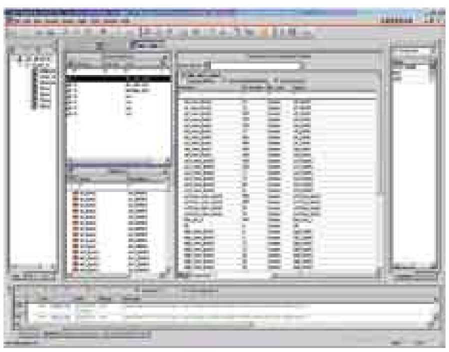

Figure 2: System Connectivity Manager

VIRTUAL SYSTEM INTERCONNECT (VSIC) MODELS

An integrated graphical and topological interconnect modeling and simulation capability provides the ability to create and explore the signal integrity (SI) performance of proposed system-level connectivity. Embedded simulation capability provides time and frequency domain interconnect simulation, including industry-standard S-Parameter models. A full 3D quasi-static field solver further provides the extraction and creation of detailed, accurate geometric IBIS, RLGC or S-Parameter models of complex 3D interconnect structures. (*See Figure 3.*)

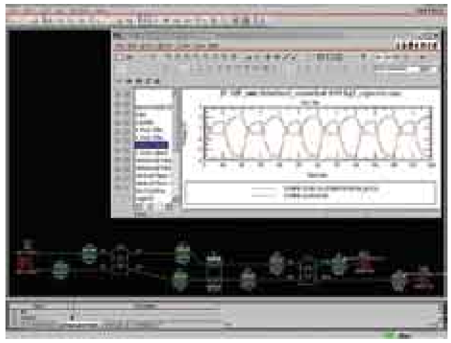

Figure 3: Virtual System Interconnect Models

I/O PLANNER

The IC die abstract I/O planner provides the definition and optimization of co-design die bump matrix, I/O pad ring/array through connectivity assignment, I/O placement, and redistribution layer (RDL) routing. It can create either a die abstract from scratch, or load an abstract from the digital IC design team (LEF/DEF or OA), and then optimize it in the context of the SiP substrate as well as other IC die in the design. The I/O planner is based on Encounter technology, ensuring it is 100 percent compatible with the chip design team's IC tools and provides complete IC technology file compliance. (*See Figure 4.*)

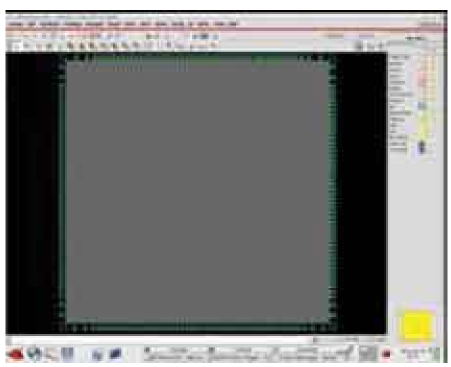

Figure 4: I/O Planner

SUBSTRATE FLOORPLANNER

The floorplanner allows the physical prototyping and evaluation of various substrate-level SiP implementation concepts. It provides a full rules-driven, connectivity-based capability that ensures a correct-by-construction approach. The die abstracts, discrete components, and connectivity and constraint data is used to build the physical SiP implementation.

The SiP architect can then use the graphical, intuitive editing tools to construct and evaluate critical sections of the design. (*See Figure 5.*)

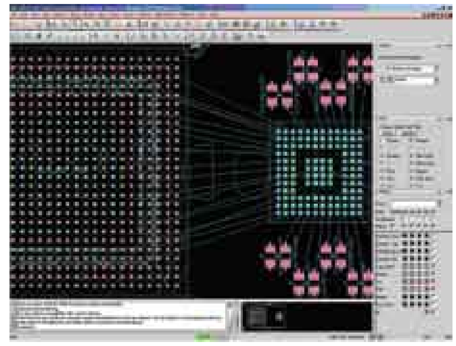

Figure 5: Substrate Floorplanner

3D DIE STACK EDITOR

The die stack editor provides a 3D construction environment for assembling complex die stacks which can include spacers, interposers and die attach methods such as wirebond and flip chip. (*See Figure 6.*)

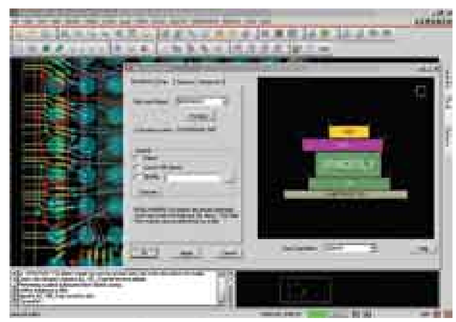

Figure 6: 3D Die Stack Editor

3D DESIGN VIEWER

The Cadence 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond DRC solution for complex IC package designs. It allows users to visualize and investigate an entire design, or a selected design subset, such as a die stack or complex via array. It also provides a common reference point for cross-team design reviews. (*See Figure 7.*)

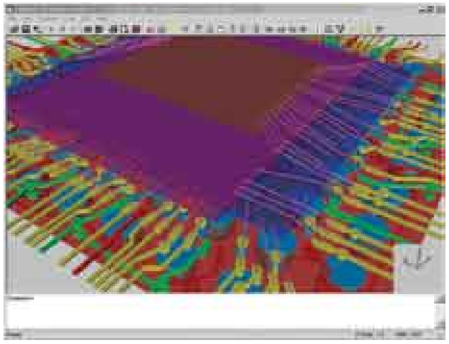

Figure 7: 3D Design Viewer

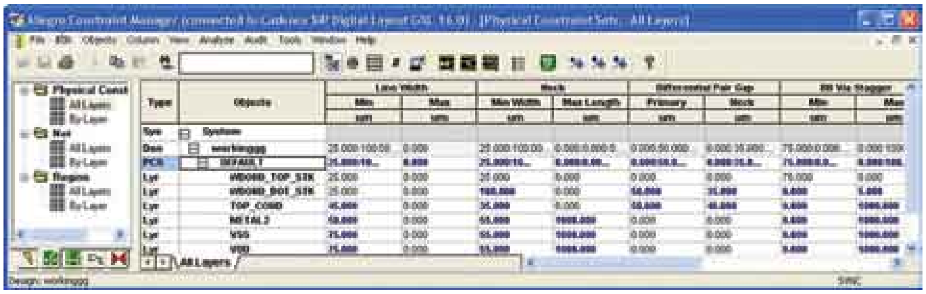

Figure 8: Integrated Constraint Management

INTEGRATED CONSTRAINT MANAGEMENT

The spreadsheet based Integrated constraint management system provides the definition, application, and management of interconnect constraints and topologies at the physical prototyping and implementation level. Designers can import constraints and apply them to industry-standard buss protocols—such as PCI-Express and DDR2—through hierarchical interconnect topology templates that are available from Cadence as well as various IC vendors. (*See Figure 8.*)

EMBEDDED 3D FIELD SOLVER AND SIMULATION TECHNOLOGY

Seamless integration with quasi-static 3D field solver technology and SPICE-based simulation engines from within the physical SiP design environment enable modeling and simulation of package interconnect, without the time-consuming setup of stand-alone point tools. Engineers can quickly check tradeoffs to the physical design to ensure that electrical requirements are not compromised. Integration of analysis and design technology also allows analysis tasks that were formerly done by package SI experts to be shared by a broader group within the SiP design community. (*See Figure 9.*)

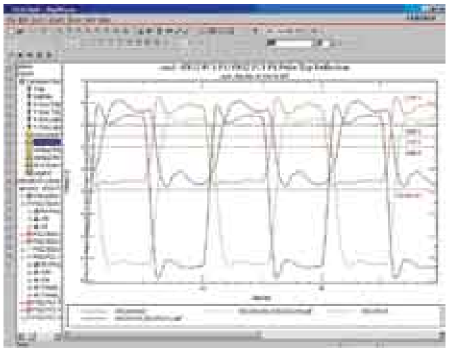

Figure 9: Embedded 3D Field Solver and Simulation Technology

PACKAGE MODELING FOR SYSTEM LEVEL ANALYSIS

Creation of IBIS, RLC, or Cadence DML interconnect models is easily accomplished, either for a selected set of nets or for the entire package. Design teams can then easily re-use these models at the system level to ensure that package effects are properly considered when optimizing PCB cost/performance tradeoffs.

INTEGRATION WITH CHIP-LEVEL IR DROP ANALYSIS

Creation of package power and ground RLC models that can be automatically consumed by IC core IR drop analysis (static and dynamic) using Cadence VoltageStorm®. (*See Figure 10.*)

SUBSTRATE EDITOR

The substrate place and route editor allows the package layout designer to physically implement a SiP design based on the final chosen concept, including all levels of manufacturing preparation prior to mask creation. It provides a full rules-driven, connectivity-based capability that ensures a correct-by-construction approach backed by a comprehensive design and assembly rule checking environment. The die abstracts, discrete components, and connectivity and constraint data are used to build the physical SiP implementation. The package layout designer can then use intuitive graphical editing tools to implement the design and prepare it for

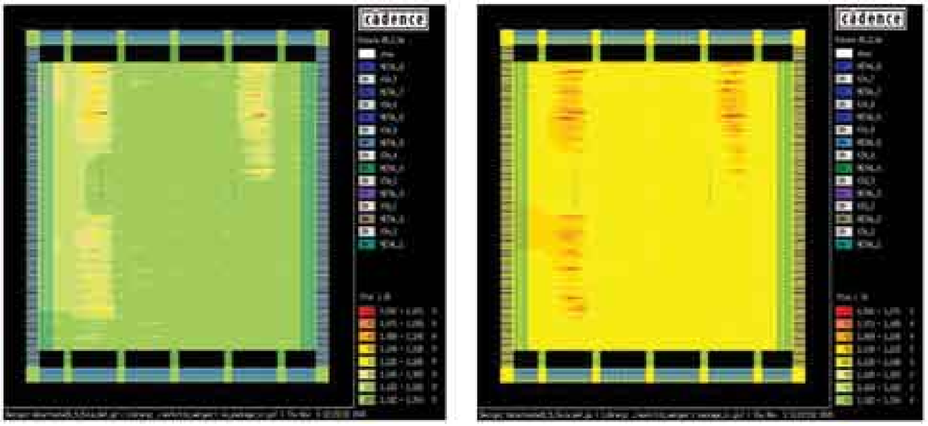

Figure 10: Integration with Chip-Level IR Drop Analysis

manufacture. It also supports all packaging methods: PGA, LGA, BGA, micro-BGA, and chip scale, as well as flip-chip and wirebond attach methods. An embedded, push-button, full 3D quasi-static field solver provides the extraction and creation of detailed, accurate geometric RLC or S-Parameter package simulation models for use during PCB design. (*See Figure 11.*)

ARC/BDR CHECKING

A comprehensive assembly and manufacturing rule checker provides over 35 SiP specific checks. Check can be executed as a check-group, or individually, or as a custom selection. Check results appear in the Constraint Manager DRC tab and as graphical markers in the design. (*See Figure 12.*)

AUTO/INTERACTIVE WIREBONDING

New, highly productive environment provides fast, powerful and flexible bondshell creation and editing. Constraint/rules driven automatic bondfinger array placement can be used with staggered die pads, multiple bond levels, multiple bond rings, and both symmetrical and non-symmetrical designs. For fast initial what-if prototyping of single or multiple die stacks the "autobond" feature instantly creates a symmetrical bondshell pattern including power and ground rings. Unique push and shove bondfinger editing enables extremely complex bondshells to be developed in minutes, delivering unparalleled capability and productivity. All this is supported by extensive wirebond rules and constraints that provide real-time design feedback. Wirebond attached die flags and power/ground rings can be quickly created, edited, and optimized for multiple voltage supplies. (*See Figure 13.*)

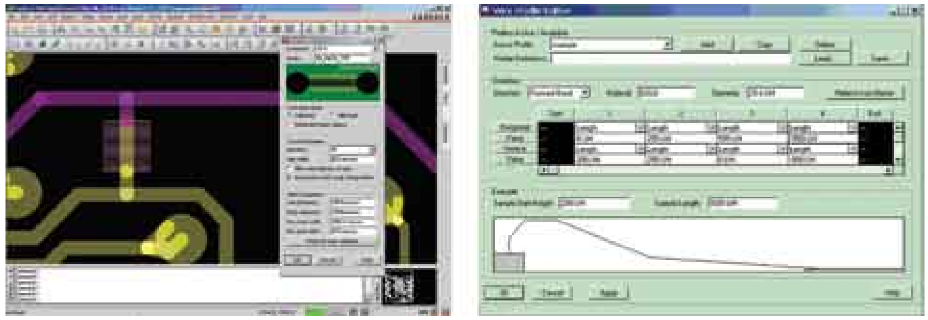

Figure 11: Substrate Editor

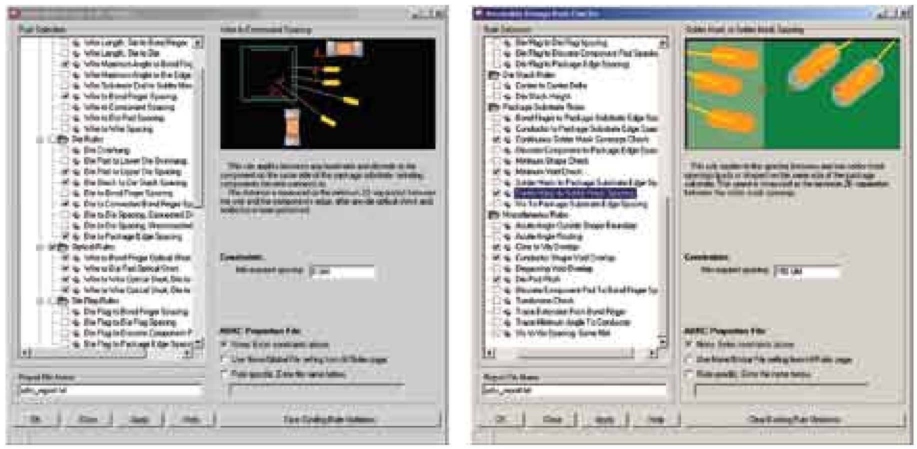

Figure 12: ARC/BDR Checking

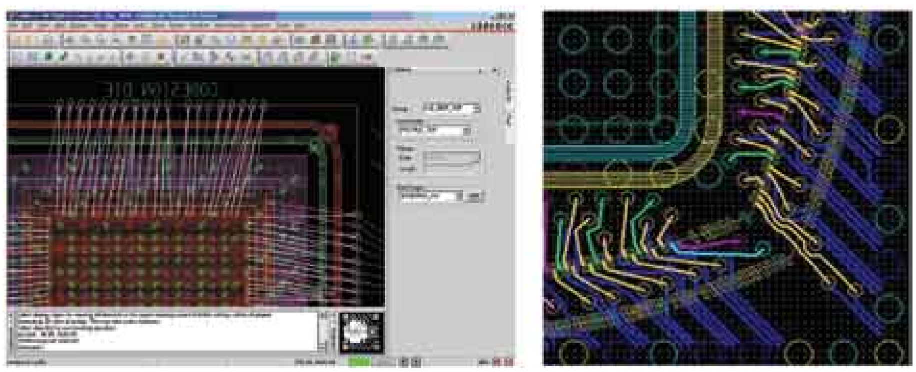

Figure 13: Auto/Interactive Wirebonding

PRODUCT FEATURES

	SiP DIGITAL ARCHITECT GXL	SiP DIGITAL ARCHITECT XL	SiP DIGITAL LAYOUT GXL	SiP DIGITAL SI XL	SiP RF ARCHITECT XL	SiP RF LAYOUT GXL
FRONT-END DESIGN CREATION FEATURES						
Virtuoso Analog Design Environment, schematic/layout integration and flow					•	
Substrate-level embedded RF passive synthesis					•	
System Connectivity Manager with logical co-design objects	•	•				
Full SiP LVS (substrate and ICs)	•	•			•	
SIGNAL INTEGRITY FEATURES						
SigXplorer topology editor and simulator (pre-route capabilities)	•			•		
SigXplorer topology editor and simulator (pre- and post-route capabilities)				•		
S-Parameter interconnect modeling and SI simulation	•			•		
Source synch and serial interface simulation	•			•		
3D PCB full-package simulation model creation	•		•	•		•
Quasi-static 3D extraction/modeling engine	•			•		
Co-planar coupling extraction	•			•		
Spectre transistor-level simulation engine	•			•		
Channel analysis for high-capacity SI simulation	•			•		
Etch back stub effects simulation	•			•		
Package/pin delay length report	•		•	•		•
SUBSTRATE DESIGN FEATURES						
Constraint Manager (electrical/physical and DRC)	•	•	•	•		•
Import/export APD (.mcm) database	•		•			•
Interactive (i/a) and automatic component (packaged and bare die) placement i/a only	•		•	i/a only		•
Auto/interactive wirebonding including rapid autobond	•		•	•		•
User-definable wirebond model profiles including XML import	•		•	•		•
Full and partial design connectivity assignment and optimization (router-based, closest match, interactive and constraint-based)	•		•	•		•
Interactive and automatic interconnect routing (free angle and multi-layer orthogonal)	•		•	•		•
On-line soldermask checking			•			•
Recursive breakout pattern creator (flip-chip and wirebond)	•		•			•
Static-style screen rulers						•
ADVANCED DESIGN FEATURES						
I/O planning co-design editor (using LEF/DEF and OA 2.2)	•		•			•
Hierarchical GDSII output			•			•
Embedded RF passive creation and editing						•
3D Design Viewer and 3D wirebond DRC	•		•	•		•
3D Die Stack Editor	•		•			•
Interconnect cline spreading			•			•
BGA editor	•		•	•		•
HDI via structure support	•		•	•		•
DFM PREPARATION/OUTPUT						
Die/BGA footprint compare using DEF/OA/.TXT	•		•			•
Filled shapes (metal) creation and editing			•	•		•
Design documentation (dimensioning, annotation)			•			•
Assembly and back-end DRC system			•			•
Etch back of plating traces			•			•
Plating bar generation			•			•
Manufacturing/documentation export/import capabilities (stream, dxf, AIF)			•			•
Substrate mask output (Gerber, GDSII)			•			•
Full design-status reporting capabilities	•		•	•		•
Waived DRCs (creation and reporting)	•		•	•		•
Degassing of filled metal shapes			•			•
Thieving (metal area balancing)			•			•

SPECIFICATIONS

SYSTEM REQUIREMENTS

- OpenGL graphics compliance with a minimum of 64MB of dedicated memory

PLATFORM/OS

- Windows XP, Vista Enterprise
- Solaris
- Linux

INTERFACES

- LEF/DEF 5.1 to 5.6
- OA 2.2
- Verilog

THIRD-PARTY SUPPORT

- Optimal O-wave and Powergrid for full wave post-layout extraction and power delivery modeling

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

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