DATASHEET

SMIC-CADENCE LOW POWER DIGITAL REFERENCE FLOW FOR ENERGY-EFFICIENT 130 NANOMETER SOC DESIGNS

An Encounter-based solution, the SMIC-Cadence Low Power Digital Reference Flow employs the widely-used Artisan library to facilitate the design and development of low-power, energy-efficient SoCs.

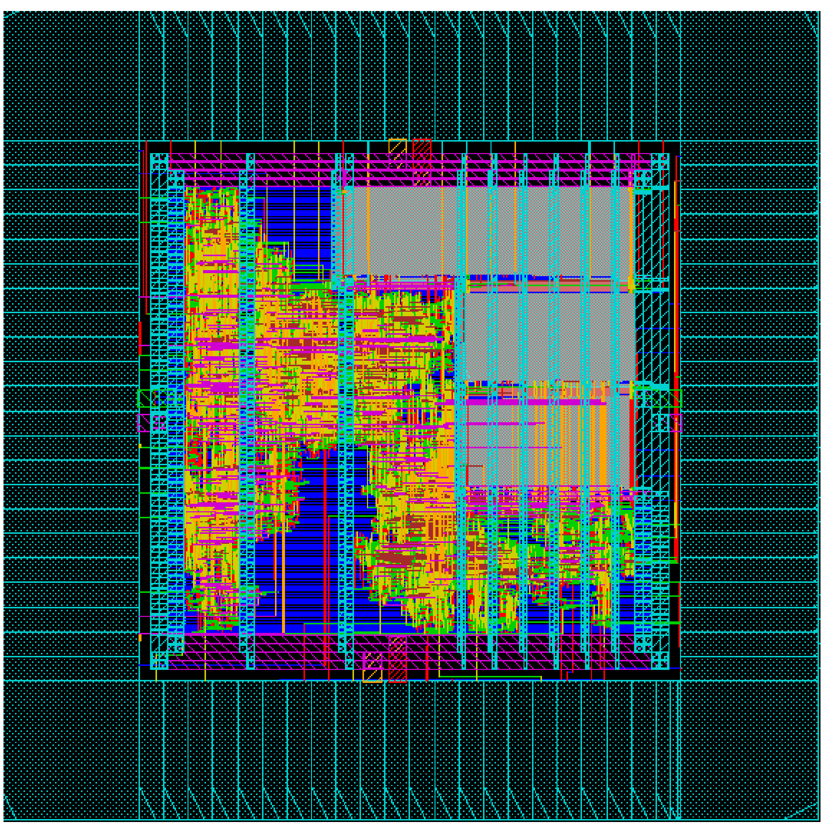

Figure 1: Based on an open-source processor, the SMIC-Cadence Low Power Digital Reference Flow offers a validated starting point in silicon for the creation of energy-efficient, sub-130 nanometer SoCs.

Validated in silicon at 130nm, the SMIC-Cadence Reference Flow leverages the capabilities offered by Cadence RTL Compiler to achieve concurrent optimization of timing, area utilization, and power. The global optimization process across these three key areas delivers better overall performance and superior power utilization.

Providing a tested and predictable path to silicon, the SMIC-Cadence reference flow is based on an open-source processor that delivers a validated starting point for designers developing power-efficient 130nm SoCs. Optimized for the SMIC .13µm Generic Process, the flow uses ARM's Artisan Library, the SMIC IO Library, and other intellectual properties (IP) to deliver high Quality of Silicon (QoS). All key processes in the flow are optimized, including power utilization, timing closure, signal integrity, and area reduction.

The market for advanced handheld and portable devices is expanding exponentially, creating a demand for powerful and energy-efficient SoCs. The performance demands of next-generation audio/video handhelds and other compact multimedia devices require a combination of performance with the highest levels of energy efficiency to reduce heat and prolong battery life.

To achieve this goal, the SMIC-Cadence reference flow delivers a low-power solution focused on efficient energy utilization. The flow utilizes intellectual property (IP) from Artisan, including high-threshold and low-threshold libraries. These libraries are used in conjunction to optimize the power utilization of SoC designs. Encounter Multi-vth optimization is used to control leakage power by replacing low vth cells with corresponding high vth cells in non-critical timing paths, creating a more power-efficient design.

The SMIC-Cadence Low Power Digital Reference Flow enhances design team productivity and offers a faster, validated, reduced-risk path to silicon. Key Cadence technologies utilized in implementing the flow include RTL Compiler, First Encounter, Global Physical Synthesis (GPS), NanoRoute, Incisive Conformal, VoltageStorm PE, Fire & Ice QX, CeltIC, Virtuoso Chip Editor, and Assura.

FEATURES AND BENEFITS

- Validated as fully compatible with the leading-edge SMIC 130nm Logic 1P8M 1.2/2.5/3.3V generic process and Artisan's 130nm standard cell library and IP
- Utilizes widely-accepted, effective Artisan libraries to streamline the SoC design process
- RTL Compiler enables timing, area usage, and power issues to be resolved concurrently, providing higher QoS levels and more efficient power utilization
- Offers comprehensive leakage power savings to facilitate the design of energy-efficient SoCs for the consumer handheld and portable markets

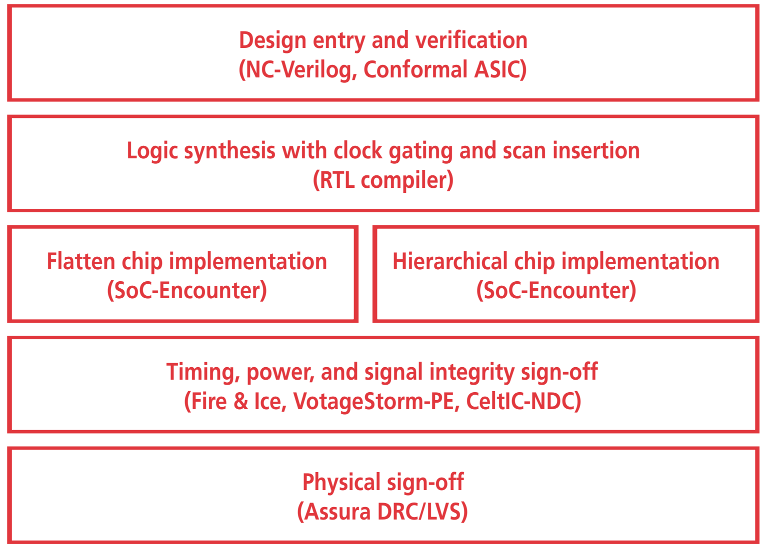

Figure 2: SMIC-Cadence Low Power Digital Reference Flow

- Multi-Vt Flow optimizes leakage power by utilizing RTL Compiler and SoC Encounter to create a balance between achieving timing convergence while maintaining leakage power at minimum levels
- VoltageStorm Professional Edition (VSPE) performs flat and hierarchical power-grid analysis and signoff of cell-based designs, such as custom ICs, ASICs, and system-on-a-chip (SOC). VoltageStorm provides SignalStorm Delay Calculation with instance-specific IR drop information, enabling timing analysis to be performed under realistic conditions

As time-to-market cycles become shorter and increasingly urgent, the need for SoC design acceleration techniques capable of meeting these time pressures becomes critical. Increased time pressure and the threat of cost overruns in both design and manufacturing has heightened the urgency for uncovering and correcting potential problems early in the physical design cycle. Failed designs and production delays have the potential of causing millions of dollars in cost overruns, making the use of a complete, integrated, and reproducible RTL-to-GDSII flow essential.

To answer these challenges, the Encounter-based SMIC-Cadence Low Power Digital Reference Flow supports the creation of large, hierarchical or flat SoC designs with dynamic power optimization. Sophisticated development techniques included in RTL Compiler include clock gating, logic restructuring, and power optimization. In addition, Encounter Multi-vth optimization is used to control leakage power by replacing low vth cells with corresponding high vth cells in non-critical timing paths.

To facilitate the cost-effective development of highly-customized SoCs, Cadence and SMIC have developed and verified an open-source, sub-130nm test design (see Figure 1). The test design is based on the SMIC-Cadence reference flow, incorporating the SMIC .13µm Logic 1P8M generic process and the following libraries:

- ARM .13µm HVT SAGE-X Standard Cells (high Vth)
- ARM .13µm Generic SAGE-X Standard Cells
- SMIC IO Library (SP013D3)
- ARM .13µm Generic High Speed/Density Single-Port SRAM
- ARM .13µm Generic High Speed/Density Diffusion ROM

SMIC-CADENCE LOW POWER DIGITAL REFERENCE FLOW

The SMIC-Cadence Low Power Digital Reference Flow provides SoC developers with a predictable and validated RTL-to-GDSII development path. Based on the complete and tightly integrated Cadence Encounter design and verification platform, the flow delivers a hierarchical RTL-to-GDSII solution for nanometer design processes at 130nm and below.

The SMIC-Cadence Low Power Digital Reference Flow includes the following key development and verification technologies:

LOGIC SYNTHESIS

RTL Compiler Logic Synthesis delivers higher-quality netlists in less time with less effort. This advanced synthesis solution provides several key benefits, starting with improved QoS in terms of power optimization, timing closure, and enhanced area utilization. Dramatically faster runtimes and higher overall capacity enables design teams to work more effectively. With new global optimization algorithms, Encounter RTL Compiler performs a single-pass concurrent synthesis for meeting timing, area, and power targets to create low-power, multi-million gate designs.

SILICON VIRTUAL PROTOTYPING

First Encounter-based Silicon Virtual Prototyping (SVP) is the cornerstone of the SMIC-Cadence Low Power Digital Reference Flow, providing designers with a streamlined method of validating their design assumptions and constraints. Because the SVP process delivers immediate feedback on the timing, congestion, and power consumption of the SoC, design time can be reduced by an order of magnitude from that of performing a complete place-and-route iteration.

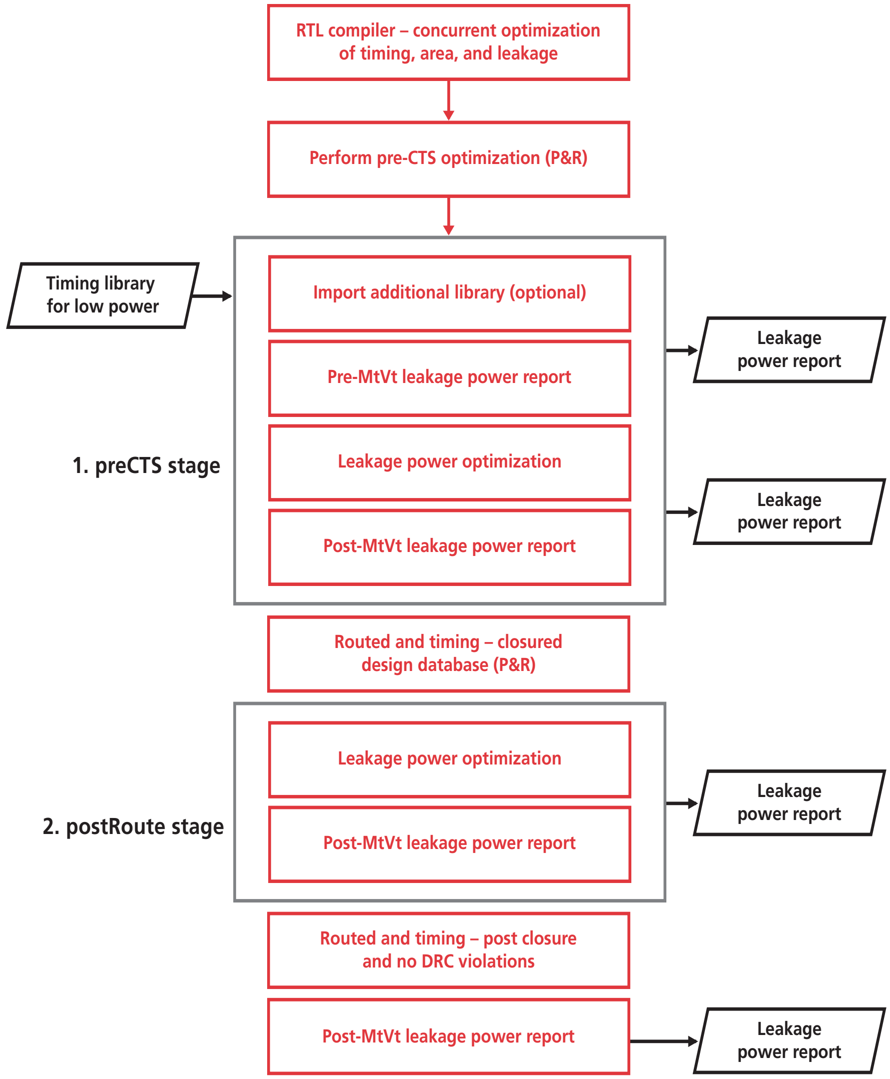

Figure 3: The Multi-Vt Flow provides a new level of visibility into leakage power optimization during the Blocks and Top-level Implementation process

HIERARCHICAL FLOORPLAN GENERATION

First Encounter uses a hierarchical methodology to facilitate chip implementation. Hierarchical floorplanning decisions can be finalized after the Silicon Virtual Prototyping phase is completed. Hierarchical Floorplan Generation defines the top-level floorplan, and blocks within that floorplan that can be implemented separately for increased design control.

EQUIVALENCE CHECKING

The Cadence Incisive Conformal logic equivalence checker is used throughout the flow to check functional equivalence of two versions of a design, enabling errors to be quickly identified and corrected.

BLOCKS AND TOP-LEVEL IMPLEMENTATION

Top-level implementation involves placement, in-place optimization, clock-tree synthesis, and routing. It follows after all blocks are implemented, and where standard block models are generated. Physical synthesis can be launched for timing closure of the most difficult blocks.

- First Encounter Global Physical Synthesis combines silicon virtual prototyping with high-performance physical synthesis capabilities that leverage Cadence RTL Compiler's patented global-focused synthesis technology. Unlike traditional physical synthesis approaches that optimize a single logic path at a time, GPS is capable of optimizing the timing of multiple paths simultaneously. This approach reduces the amount of time and effort required to reach design convergence. GPS is capable of optimizing both RTL-to-placement and netlist-to-placement.
- Multi-Vt Flow is a integral part of the leakage power optimization process. The process starts with concurrent optimization of timing, area and power in RTL Compiler. The leakage power optimization technology is implemented with SoC Encounter, and then a multi-step process is conducted to complete the top-level implementation. A balance is reached between achieving timing convergence while maintaining the leakage power at minimum levels. The unsolved timing violations are then addressed to further optimize the SoC design.
- Signal Integrity (SI) Closure is achieved by the SI-aware NanoRoute routing solution, which features built-in “design for manufacturability” (DFM) capability. Routing resulting from NanoRoute has minimal signal integrity violations and has been demonstrated to meet timing and manufacturability constraints in many tapeouts. The SI closure loop, which is performed using CeltIC-NDC, eliminates any remaining SI violations from the design.

CHIP ASSEMBLY AND SIGN-OFF

The SMIC-Cadence Low Power Digital Reference Flow uses the industry's most accurate sign-off extractor-Fire & Ice QX. This provides a well-proven solution for accurately validating the timing of nanometer designs while enabling detailed Signal Integrity verification. The flow also uses the industry standard power grid verification tool-VoltageStorm PE -to ensure that power requirements are met. Equivalence Checker is then run to complete the SoC assembly and sign-off process.

CHIP FINISHING

Fully interoperable with the Cadence Encounter digital IC design platform, Virtuoso Chip Editor Physical provides high-performance editing for full-chip finishing tasks on even the largest designs, dramatically reducing the time required for tapeout tasks. Physical verification is performed by Assura to identify design rule errors prior to taping-out to manufacturing.

FOR MORE INFORMATION

To learn more Find out more about how Cadence and SMIC are partnering to facilitate your success by visiting: **http://www.cadence.com/partners/foundry_program/XXX.aspx** or by contacting us at: foundry_support@cadence.com.

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