

CADENCE SoC FUNCTIONAL VERIFICATION KIT

To reduce risk, achieve predictable verification closure, and deliver innovative products on time, engineers need automated verification process management, IP reuse, and the latest verification methodologies. The Cadence® SoC Functional Verification Kit offers design and verification teams a comprehensive solution, tailored to ARM-based devices, to ease the adoption of new verification technologies and methodologies. The Kit provides an interactive view of the proven Cadence Incisive® Plan-to-Closure Methodology, delivering more efficient verification planning and execution.

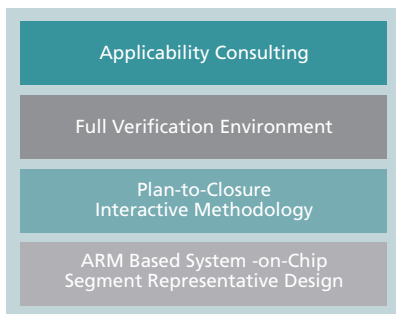


Figure 1: Cadence SoC Functional Verification Kit

With unforgiving market windows and ever-increasing demand for more functionality and performance packed into each new SoC, design and verification engineers face a paradox, especially in wireless and consumer applications: delivering better products requires incorporating new technologies, which may introduce risk to the design and verification process. As these challenges escalate, engineers need a verification process that is easy to adopt, uses

the latest techniques, boosts productivity through automation and IP reuse, and increases predictably to meet their delivery goals.

CADENCE SoC FUNCTIONAL VERIFICATION KIT

Jointly developed and endorsed by Cadence and ARM, the Cadence SoC Functional Verification Kit offers a comprehensive verification solution specifically tailored for engineers developing ARM-based SoC designs. The Kit contains verification methodologies and flows, a realistically challenging segment representative design (SRD), the Incisive Plan-to-Closure Methodology, and reusable verification IP—and it's the industry's first kit to utilize an interactive methodology navigator that drives a coverage-driven verification environment (See Figure 1.). The Kit highlights methodology options and tradeoffs for customers

moving to the next level of verification productivity, independent of design or verification language choice.

Combined with the Incisive platform's verification process automation (VPA) technology and IP, the Cadence SoC Functional Verification Kit addresses the verification of both hardware and software from block to chip to system levels. It guides engineers through the following processes and flows to provide a streamlined path from verification planning to closure:

- Real-world, segment representative design to prove and demonstrate flows and methodologies
- Pre-built verification environment and language-neutral verification environment
- Advanced verification architecture, maximizing reuse from block to chip to system level
- Automated verification planning and management

- Architectural modeling and analysis for early HW/SW co-verification
- Low-power functional verification flow to verify low-power attributes at the RTL level
- Assertion-based verification for formal analysis, simulation, acceleration, and emulation
- Testbench automation to address challenging corner-case bugs
- Use of certified ARM® AMBA™ verification IP and protocol compliance
- Embedded software IP used in HW/SW co-verification for both simulation and hardware-assisted verification flows
- Transaction-based acceleration for high-performance RTL verification
- In-circuit emulation for system and software validation as well as HW/SW co-verification
- Methodology workshop modules covering all aspects of the Kit in a Plan-to-Closure format, utilizing the breadth of Incisive technologies

The Cadence SoC Functional Verification Kit demonstrates three primary verification flows on an ARM968-based wireless segment representative design (See Figure 2.). This platform consists of the ARM968 processor and multi-layer AHB switch fabric, memory subsystems, USB 2.0, 802.11 WLAN, and a host of Cadence interface peripherals devices.

The Kit contains documented best practices and “golden” executable verification plans provided as real-world examples embedded within the Kit. It utilizes the proven and language-neutral Universal Verification Component (UVC) standard applied to multiple design blocks within the environment. The UVCs provided consist of executable compliance verification plans; assertions for formal analysis, simulation, and acceleration; compliance management utilities; and transaction-based interface acceleration and common testbench reuse for hardware-assisted verification.

INTERACTIVE METHODOLOGY NAVIGATION

The Cadence SoC Functional Verification Kit contains a first-of-its-kind interactive methodology approach with an easy-to-use mouse-driven Kit navigator (See Figure 3.), which allows you to navigate to just the portion of the Kit you want to understand. This approach maximizes comprehension and learning, making a transition to more advanced verification simpler than ever. For design teams

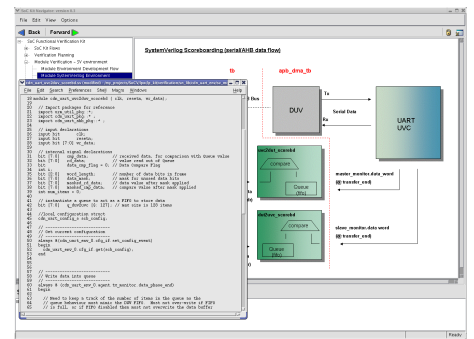


Figure 3: Interactive Methodology Navigator

moving from directed tests, to advanced verification teams looking to maximize their verification effectiveness, the Cadence SoC Functional Verification Kit allows you to optimize your learning based on what you know today, and offers an evolutionary approach to ease adoption of new verification technologies and methodologies (See Figure 4.).

POWERFUL ENGAGEMENT PROCESS

Design and verification teams can use the segment representative design platform and interactive methodology navigator as a basis to understand the coverage-driven verification techniques within the Incisive Plan-to-Closure Methodology. Then, with the assistance of application consulting, they can map the demonstrated techniques, technologies, and IP to their own environment. The onsite applicability consulting is the final phase of a highly

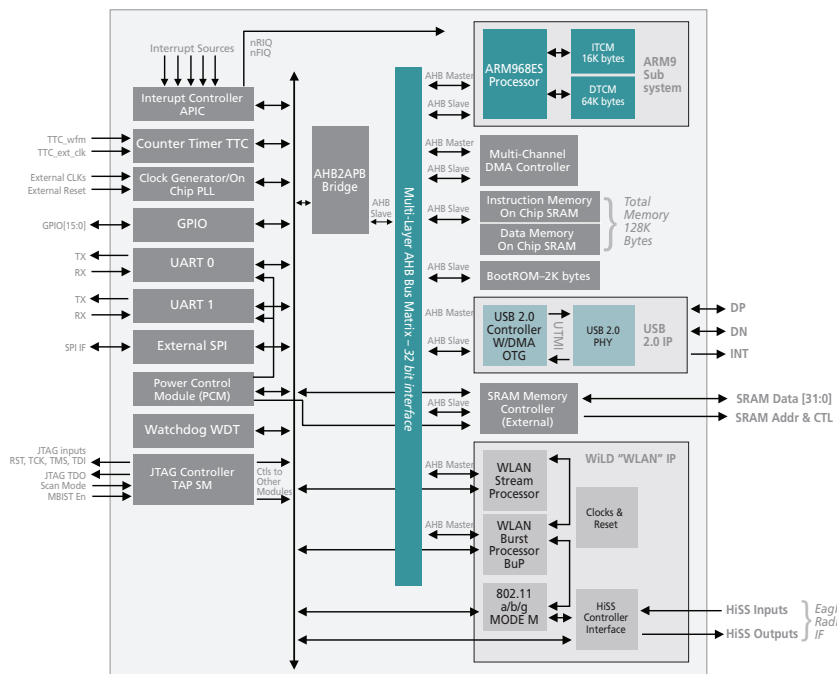


Figure 2: ARM968 Wireless Segment Representative Design

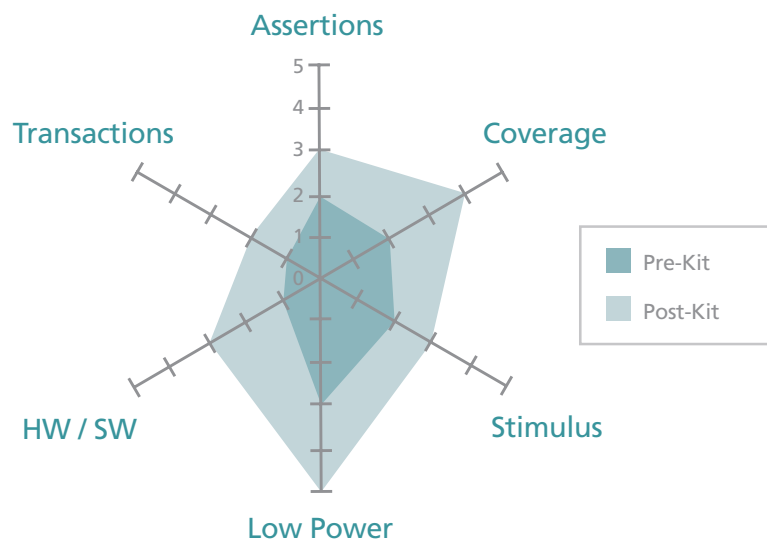


Figure 4: Improved Verification Effectiveness using Cadence SoC Functional Verification Kit Flows and Methodologies.

predictable and proven engagement process, designed to deliver maximum benefit and user experience in the shortest amount of time. This step-by-step approach allows a team to absorb and understand a wide array of technologies that can optimize the verification process and address the unique challenges they face in verifying SoCs.

Cadence utilizes its pre-engineered workshops to deliver methodology expertise to Kit users. The methodology is efficiently organized into a number of workshop modules that are delivered during the applicability consulting phase of the engagement. Workshops cover all aspects of the verification process and teach how to utilize the methodology to maximize productivity. Each applicability consulting engagement is tailored to the customer's specific verification challenges.

At the end of the Kit engagement, customers designing ARM-based SoCs can increase the predictability of meeting product development milestones, lower adoption risks, and achieve their time-to-market goals.

BENEFITS

- Eases adoption of new verification technologies and methodologies
- Increases predictability by automating the verification management process
- Improves learning productivity and comprehension by utilizing interactive methodology navigation
- Ensures process management and AMBA/ USB specification compliance via executable verification plans
- Reduces risk by leveraging the industry-proven Plan-to-Closure Methodology
- Enables verification IP reuse across block, chip, and system levels, enabling more efficient verification planning and execution
- Ensures product quality by verifying both hardware and software simultaneously
- Improves productivity and ease-of-adoption within a scalable environment
- Based on IEEE-standard languages: *e*, SystemVerilog, SystemC®, Verilog®, VHDL

1. Third-party and Cadence design IP require separate license to use within a production design

KIT COMPOSITION AND INTEGRATION

The Cadence SoC Functional Verification Kit includes the following:

- Three validated and documented flows: Architecture, Block-to-Chip, and System
- Documented use and examples for Palladium® technology in the system flow, showing both transaction-based acceleration (TBA) and in-circuit emulation (ICE)
- Kit IP including verification components (executable verification plans), software IP, (including drivers and test software), and peripheral design IP, available in source format ¹
- Low-power CPF-based flow and usage guidelines, including formal assertion library, software test code, and power control module in source format
- Full ARM968-based segment representative design including third-party IP blocks for USB 2.0 and 802.11 wireless LAN ¹
- Step-by-step interactive methodology navigator and "golden" examples (navigator provided in source format)
- 'Simulate' and 'Coverage' automation scripts
- Onsite pre-defined expert applicability consulting designed to map a portion of the customer design into the Kit and provide hands-on experience with methodologies and new verification techniques
- Workshop content:
 - Kit Introduction and ARM Reference Design
 - Planning and Implementing the Incisive Plan-to-Closure Methodology
 - Transaction-Level Modeling
 - Acceleration and In-Circuit Emulation
 - *e* Verification Environment
 - SystemVerilog Verification Environment

- Mixed-Language Integration
- Formal and Assertion Analysis
- Low-Power RTL Verification
- Compliance Testing
- Verification Component Creation
- Scenario Building and Generation

The Cadence SoC Functional Verification Kit relies on and integrates with the following Cadence Incisive platform technologies (45-day temporary license included):

- Incisive Enterprise Simulator
- ESL Option for Incisive Enterprise Simulator
- Incisive Enterprise Manager
- Incisive Formal Verifier
- Incisive Plan-to-Closure Methodology
- Incisive AHB and USB Universal Verification Components (UVCs)

Additional software needed to run the Kit include:

- ARM968 Processor Models (DSM and CCM)
- ARM RealView Development System (RVDS) or
- GNU Software Debugger Option (GCC)

Environment and platform:

- Local: The Kit is delivered as a tarball operating within a Linux environment

- Remote: Cadence offers a “Collaboration Chamber” (a pre-configured and fully functional set of Cadence technologies, IP and the Kit) for test drives

CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

For more information about this and other products contact:

1.800.746.6223

or log on to:

www.cadence.com/contact_us

cadence™

Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS

2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 (*within US*)
+1.408.943.1234 (*outside US*)
F: +1.408.943.5001
www.cadence.com