



Open Verification Methodology (OVM)

Delivering the SystemVerilog
Interoperability Promise



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SystemVerilog Promise Partially Achieved

Open methodology was missing

- IEEE 1800 standardized SystemVerilog language
- Multiple class libraries restricted interoperability
 - Different language subsets
 - Tied to single simulator
 - Incompatible verification IP (VIP) interfaces
- Multiple methodologies restricted reuse
 - Prohibitive licensing limited multi-vendor support
 - Incomplete and incompatible technology restricted VIP plug 'n' play
 - Communication, messaging and synchronization, test-writer interface, etc.
 - Loose multi-language support made RTL/TLM integration difficult
 - Transaction-level modeling (TLM) standard for model communication

Open Verification Methodology (OVM)

Delivers the SystemVerilog interoperability promise

- First truly open, interoperable, and proven verification reuse methodology
 - Framework for reusable VIP and testbench
 - Includes guidelines for using the class library
 - Scalable to system level verification
- Open-source IEEE 1800 class-library
 - Runs on any compliant simulator
 - Provides building blocks (objects) and common set of verification related utilities
 - True open-source license (Apache 2.0)
- Jointly developed
 - Built from Cadence's Incisive Plan-to-Closure class-based URM library and methodology
 - Built from Mentor's AVM for base class library





Superset of AVM and URM

Creates shared vision for testbench methodology

- Proven using best practices from >10 years of experiences
- Backward compatible with AVM 3.0 and URM 6.2
- On-going, collaborative development committed by both Mentor and Cadence

OVM

Open, unified class library and methodology for interoperable VIP

- Project-to-Project Reuse
- Block-to-System Reuse
- Coverage-Driven
- Environment Configuration
- Incremental Adoption
- Multi-Layered Sequences
- TLM Communication
- Common Messaging



OVM's Unique Technical Advantages

Openness combined with advanced features

- Open and interoperable
 - Proven consistent simulation behavior across vendors
- Multi-language VIP plug 'n' play in SystemVerilog, e, or SystemC
 - Enables industry-wide VIP plug 'n' play
- Most advanced, proven methodology
 - Unique multi-channel, reusable sequence generation
 - Defines fully encapsulated, reusable verification components
 - Supports module-to-system and project-to-project reuse
 - Built-in automation and testbench capabilities
- Transaction-based debugging, built-in factory, configuration, compare, copy, etc.



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