



University Information & Software Selection Form

University Program 2008

Instructions

Please fill out this form completely and return all pages along with the signed Policies document and a Purchase Order to: **Cheryl Mendenhall by fax or email**. You must also have an authorized university representative sign the License Agreement.

Cadence Contact Information:

Cheryl Mendenhall

University Program Coordinator

Cadence Design Systems, Inc.

4516 Seton Center Parkway, Suite 300

Austin, TX 78759

Website: http://www.cadence.com/support/university/ww_usp.aspx

Phone: (512) 342-5350

Fax: (512) 342-5021

Email: cherylm@cadence.com

University Information

Date: _____

University: _____

Licensing Professor: _____

Dept: _____

Address: _____

Phone: _____ **Fax:** _____

Email: _____

Technical Liaisons

Primary: _____ **Secondary:** _____

Dept: _____ **Dept:** _____

Address: _____ **Address:** _____

Phone: _____ **Phone:** _____

Fax: _____ **Fax:** _____

Email: _____ **Email:** _____

A web site pertaining to your use of Cadence software is required!

URL: _____

Server Platform: SUN (Solaris) HP (HP-UX) IBM (AIX) RedHat (Linux) Windows

Configuration Information

Model: _____ **OS Version:** _____

HOST ID: _____



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Custom Integrated Circuits Bundle

Estimated number of licenses needed: _____

<u>Class or Research?</u>	<u>Title of Class or Research Project</u>	<u>Students with Cadence Access</u>
_____	_____	_____
_____	_____	_____
_____	_____	_____

The Custom IC Bundle Software Reference List:

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
Design Environment		
Virtuoso ^R AMS Designer Environment	70000	IC 6.1
Virtuoso ^R Analog Design Environment - XL	95210	IC 6.1
Virtuoso ^R Analog Design Environment - GXL	95220	IC 6.1
Design Entry		
Cadence ^R SKILL Development Environment	900	IC 6.1
Virtuoso ^R Schematic VHDL Interface	21060	IC 6.1
Virtuoso ^R Schematic Editor Verilog ^R Interface	21400	IC 6.1
Virtuoso ^R Schematic Editor XL	95115	IC 6.1
Virtuoso ^R Analog Oasis Run-Time Option	32100	IC 6.1
Layout		
Virtuoso ^R Layout Suite GXL ¹	95321	ICS 6.1.2
Cadence ^R Chip Assembly Router ²	3300	IC 6.1
RF System-In-Package (SIP)³		
Cadence SiP RF Architect - XL	SIP410	SPB 16.01
Cadence SiP RF Layout - GXL	SIP525	SPB 16.01

¹ includes CIF reader/writer and Virtuoso Stream Interface

² includes GDSII/EDIF and LEF/DEF interfaces

³ must be installed with Virtuoso



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The Custom IC Bundle Software Reference List, continued

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
Physical Verification		
Dracula ^R Graphical User Interface	365	IC 6.1
Dracula ^R Physical Verification and Extractor Suite	70520	IC 6.1
Diva ^R Physical Verification and Extractor Suite	71520	IC 6.1
Assura TM Design Rule Checker	72110	Assura 3.1.7
Assura TM Layout vs. Schematic Verifier	72120	Assura 3.1.7
Virtuoso ^R QRC Extraction –L	QRCX100	EXT 7.1
Virtuoso ^R QRC Extraction – XL	QRCX300	EXT 7.1
Assura TM Graphical User Interface Option	72140	Assura 3.1.7
Assura TM Multiprocessor Option	72150	Assura 3.1.7
Pcell Generator	PASPCG	PAS 3.1
Graphical Technology Editor	PASGTE	PAS 3.1
Generator for Assura TM compatible verification decks	PASASG	PAS 3.1
Generator for Diva ^R compatible verification decks	PASDIG	PAS 3.1
Generator for Dracula ^R compatible verification decks	PASDRG	PAS 3.1
Error Cell Generator	PASECG	PAS 3.1
Circuit Simulation		
Virtuoso ^R Schematic Editor HSPICE Interface ¹	276	IC 6.1
Virtuoso ^R Analog Design Environment GXL	95220	IC 6.1
Virtuoso ^R Spectre ^R Analog Circuit Simulator	38500	MMSIM 6.2
Virtuoso ^R UltraSim Full-chip Simulator	33500	MMSIM 6.2
Virtuoso ^R Spectre ^R RF Simulation Option for 38500	38520	MMSIM 6.2
Virtuoso ^R Analog HSPICE Interface Option ¹	32760	IC 6.1
AMS Designer with Flexible Analog Simulation	70020	IUS 6.2
Virtuoso ^R Multi-mode Simulation	90001	MMSIM 6.2
Interfaces		
Virtuoso ^R EDIF 200 Reader	940	IC 6.1
Virtuoso ^R EDIF 200 Writer	945	IC 6.1
Cadence ^R Design Framework Integrator's Toolkit	12141	IC 6.1

¹ requires additional licenses that must be obtained from Synopsys



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Digital Integrated Circuits Bundle

Estimated number of licenses needed: _____

<u>Class or Research?</u>	<u>Title of Class or Research Project</u>	<u>Students with Cadence Access</u>
_____	_____	_____
_____	_____	_____
_____	_____	_____

The Digital IC Bundle Software Reference List

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
Place & Route and Timing		
Virtuoso ^R Layout Suite GXL	95321	ICS 6.1.2
Cadence ^R Chip Assembly Router	3300	IC 6.1
Physical Verification		
Dracula ^R Physical Verification and Extractor Suite	70520	IC 6.1
Design for Manufacturing		
Virtuoso ^R QRC Extraction -L	QRCX100	EXT 7.1
VoltageStorm (gate and transistor)	VS2	ANLS 6.2
Signal Integrity		
Encounter ^R Timing System - XL	FE725	ETS 7.1
PacifiC Static Noise Analyzer for Custom Digital ICs	CM00100	PACIFIC 6.1
Encounter ^R Timing System - L	FE625	ETS 7.1
Encounter ^R Library Characterizer- XL	ELC200	ETS 7.1
Silicon Virtual Prototyping		
Cadence ^R SOC Encounter Global Physical Synthesis (GPS)	FE200GPS	SOC 7.1
Test		
Encounter ^R Test Architect XL	ET001	ET 7.2
Encounter ^R True Time Test GXL	ET002	ET 7.2
Encounter ^R Diagnostics Engine - XL	ET009	ET 7.2
Digital System-In-Product (SIP)¹		
Cadence SiP Digital Architect – GXL	SIP125	SPB 16.01
Cadence SiP Digital SI – XL	SIP215	SPB 16.01
Cadence SiP Digital Layout – GXL	SIP325	SPB 16.01

¹ must be installed with Encounter^R



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Verification Bundle

Estimated number of licenses needed: _____

<u>Class or Research?</u>	<u>Title of Class or Research Project</u>	<u>Students with Cadence Access</u>
_____	_____	_____
_____	_____	_____
_____	_____	_____

The Verification Bundle Software Reference List

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
Functional Verification		
Cadence ^R NC-Verilog ^R Simulator	28200	IUS 6.2
Cadence ^R NC-VHDL Simulator	28400	IUS 6.2
Cadence ^R NC-Sim Mixed-Language Simulator	28000	IUS 6.2
Cadence ^R Simulation Analysis Environment (SimVision)	25010	IUS 6.2
Incisive TM Enterprise Simulator	29651	IES 6.2
AMS Option to Incisive	29370	IES 6.2
Incisive Formal Verifier	23560	IFV 6.2
ESL Option for Incisive TM Enterprise Simulator	29656	IES 6.2
Verification Process Automation		
Incisive TM Enterprise Manager	EMG100	EMGR 6.2
Formal Verification		
Encounter TM Conformal GXL	CFM300	CONFRML 7.2
Synthesis		
Encounter TM RTL Compiler -XL	RC200	RC 7.2
Encounter RTL Compiler - GXL option	RC300	RC 7.2
Pre-verified, Re-usable Verification IP Components		
AMBA AHB protocol	UVC100	UVCAMBA 2.4
USB protocol	UVC101	UVCUSB 2.3
PCI Express End Point protocol	UVC102	UVCPCIE 2.3
PCI Express Root Complex protocol	UVC103	UVCPCIE 2.3
PCI 2.2/2.3 protocol	EVC1004	EVCPCI 2.2
Ethernet protocol	EVC1006	EVCETH 2.2
AMBA AXI protocol	UVC107	UVCAXI 1.4



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Silicon-Package-Board Bundle

Estimated number of licenses needed: _____

<u>Class or Research?</u>	<u>Title of Class or Research Project</u>	<u>Students with Cadence Access</u>
_____	_____	_____
_____	_____	_____
_____	_____	_____

The Packaging & Board Bundle Software Reference List

<u>Product</u>	<u>Product No.</u>	<u>Release Stream</u>
PCB Design and Layout		
Allegro ^R PCB Librarian – XL	PX3500	SPB 16.01
Allegro ^R PCB Design HDL – XL	PX3700	SPB 16.01
Allegro ^R PCB Design CIS – XL	PX3710	SPB 16.01
PCB High-Speed Analysis		
Allegro ^R PCB SI – XL	PX3100	SPB 16.01
IC Packaging		
Allegro ^R Package Designer – XL	PA6620	SPB 16.01
Simulation		
Allegro ^R AMS Simulator ¹	PS2200	SPB 16.01

¹ superset of Pspice and Advanced Analysis Option