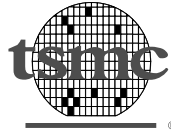


WHITE PAPER



Reference
Flow4.0
The nanometer design flow for SoC



SILICON DESIGN CHAIN COOPERATION ENABLES NANOMETER CHIP DESIGN

TABLE OF CONTENTS

Introduction 1

Nanometer Challenges 2

Manufacturability 3

Customers Win 4

TABLE OF FIGURES

Figure 1 Cadence nanometer design tools are an integral part of the TSMC Design
Reference Flow 4.0 1

Figure 2 A two-pass SI flow uses a first pass to minimize signal integrity problems and
then a second pass to correct any SI problems that may have occurred 3

1 INTRODUCTION

Shrinking process technology nodes, increasing chip complexity, more complicated design verification tasks, and shorter times-to-market have multiplied the difficulty of designing systems-on-a-chip (SoCs). It's not enough to design a chip that meets specifications — that chip must also make a successful transition to a manufacturing environment. To meet this objective, an EDA tool vendor and a silicon foundry — Cadence Design Systems and TSMC — have combined their technologies and expertise to ease the complexities of SoC design, offering specific process-related design enhancements for improved manufacturability.

Recognizing the problems with silicon design methodology over the past several years, EDA vendors and foundries have introduced products and services directly aimed at simplifying both front-end and back-end chip design. However, these efforts were often divided because of the process that separates the end of design from the beginning of chip manufacturing —silicon processing. For nanometer designs at 130 nm and below, TSMC has developed Design Reference Flow 4.0, which concentrates on back-end (post-synthesis) design and incorporates Cadence® design technologies and several design techniques to increase the probability of first-time silicon success (see *Figure 1*).

Logic synthesis	Design compiler	
Prototype/floorplan	First Encounter Ultra including PKS	
Placement		
Physical optimization		
Routing	NanoRoute	
Extraction	Star-RCXT	
Crosstalk prevention & repair	CeltIC	
IR drop	VoltageStorm	
Delay calculation	Nautilus-DC*	
Static timing analysis	PT/PT-SI	

Cadence

Synopsys

* Part of SignalStorm NDC

Figure 1: Cadence nanometer design tools are an integral part of the TSMC Design Reference Flow 4.0

A foundry-developed design reference flow created in collaboration with a key EDA vendor such as Cadence is critical to the successful design of complex SoCs. Often, customers have neither the time nor the resources to develop a design flow that is optimized for both the EDA tools used to design the chip and the specific process with which the chip will be implemented. The Cadence/TSMC cooperative effort produces the optimized design methodology that customers themselves would develop if internal resources were available to do so.

2 NANOMETER CHALLENGES

2.1 MIXED LIBRARIES BALANCE PERFORMANCE AND POWER

As process technology shrinks, designers are able to place larger numbers of transistors on a single silicon chip. At 90 nm, static power dissipation—due to transistor leakage current even when the transistors are turned off—can become a significant, or even dominant, component of total chip power dissipation. Foundry processes offer transistors with multiple threshold voltages (the threshold being the voltage level at which a device turns on). 130 nm and 90 nm TSMC processes offer three different thresholds—high, nominal, and low. The lower the threshold voltage (V_T), the sooner a device will turn on and the faster it will switch a signal. However, a lower V_T also means higher leakage through a “turned-off” device. Designers are faced with a paradox—use low V_T transistors for higher speed and high V_T transistors for lower power.

With Reference Flow 4.0, TSMC offers a guideline to minimize leakage current. Designers use high-speed (low V_T) transistors for the entire chip during the initial front-end design flow, specifically logic synthesis and optimization. This corresponds to using the fastest cell library available for the target process, with the designer optimizing the chip for timing and area. TSMC has developed cell libraries based on the ISO 9000 standard, optimized for yield and manufacturability. These libraries are verified by Cadence, who also distributes the libraries.

The cell libraries are pre-qualified for a target process and include features such as antenna diodes in flip-flops to enforce antenna design rules. After back-end placement and routing followed by parasitic extraction and timing analysis with Cadence Encounter™ digital IC design platform technology, the designer can identify timing paths exhibiting positive timing slack (paths that are faster than required for meeting the chip's timing specification).

Paths with positive timing slack show where the designer can substitute high V_T transistors for low V_T transistors, which reduces leakage current at the cost of some speed reduction on that path. Substituting high V_T for low V_T transistors does not change the chip's layout. Through repeated substitution and static timing analysis, the designer can meet timing specifications, but with a significant power reduction. Using this technique, TSMC has observed reduction in standby power by a factor of five or more and in dynamic power by a factor of two or more. The Encounter platform supports a comprehensive power strategy, including low-power optimization techniques—such as clock gating and operand isolation (sleep mode)—that are supported during the synthesis phase. Leakage power is optimized after synthesis. TSMC unique multithreshold voltage cells are supported, allowing low-threshold cells to be selected for critical paths and high- or standard-threshold voltage cells for non-critical paths, which saves subthreshold leakage power. In addition, comprehensive and accurate power analysis is available through the use of Cadence VoltageStorm® power grid verification.

2.2 DEALING WITH SIGNAL INTEGRITY ISSUES

Another serious obstacle for nanometer chip designers is meeting signal integrity (SI) specifications because of the increased contribution and sensitivity of wires. SI problems manifest themselves in several ways, including crosstalk and electromigration limitations.

At 130 nm, crosstalk problems increase by an order of magnitude over what occurs at 180 nm. You cannot correct for crosstalk violations after physical design is completed. You have to analyze crosstalk and correct problems using a reliable crosstalk analysis engine, such as the Cadence CeltIC™ signal integrity analyzer, during placement and routing operations.

Designers use Encounter design technologies within Reference Flow 4.0 during two operational flows—an SI prevention pass followed by an SI repair pass—that comprise wire-driven optimization of the chip's physical implementation (see *Figure 2*).

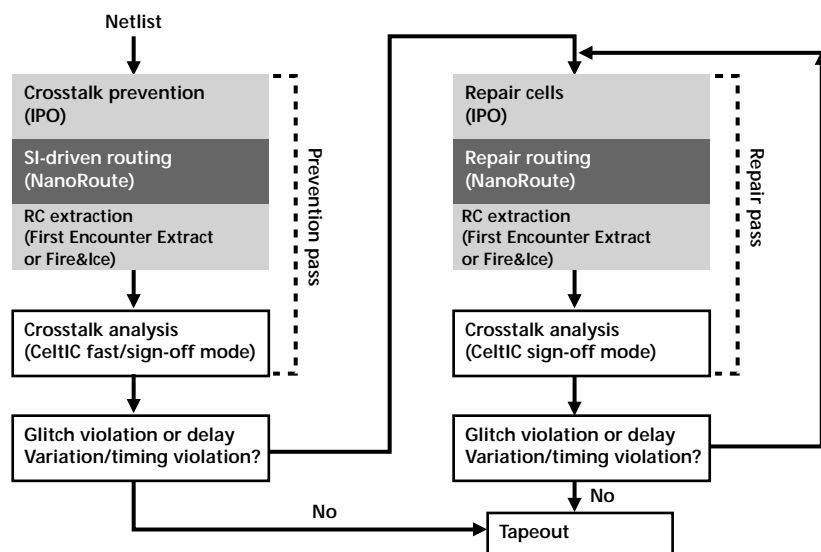


Figure 2: A two-pass SI flow uses a first pass to minimize signal integrity problems and then a second pass to correct any SI problems that may have occurred

Within the Cadence Encounter environment, the NanoRoute™ unified routing and physical optimization solution performs concurrent timing analysis and SI-driven routing to minimize SI problems. The CeltIC analysis tool then reviews the RC-extracted file from the placed and routed chip and analyzes the chip's crosstalk and other SI behavior. The Encounter platform then modifies suspect cells and, using with NanoRoute technology, repairs problematic routes to generate a chip layout that meets the SI specifications, verified by running another RC extraction operation and CeltIC analysis. The Encounter signal integrity flow within Reference Flow 4.0, including prevention and repair passes, is automated, which assures designers that their results are of signoff quality for SI compliance.

Using CeltIC cell-level signal integrity analysis within the Encounter platform is critical for successful designs that are SI-compliant. The CeltIC signal integrity analyzer detects both crosstalk-induced delay and glitch failures using a combination of cell-based and transistor-based models, resulting in Spice-level accuracy. The tool then automatically creates noise repairs for the place-and-route operations, reporting one-to-two orders of magnitude fewer false glitch violations that hinder normal design and verification tasks.

Also important for nanometer designs is detecting IR drop in the chip's power grid that can result in supply-voltage drop and ground bounce. Both effects can be major contributors to SI problems. Designers use the VoltageStorm power grid verification solution in Reference Flow 4.0 — after block placement, but prior to detailed signal routing — to detect IR drop in the power grid and guide the correction of potential noise problems. They can then use VoltageStorm power grid exploration capabilities to fix power distribution problems before moving into detailed signal routing.

3 MANUFACTURABILITY

Manufacturability used to be an afterthought for chip designers. However, shrinking process technologies are forcing chip designers to consider more constraints within the design flow that deal directly with manufacturing issues and increasing chip yields. TSMC Reference Flow 4.0 supports several yield-enhancement techniques, including process variation modeling; dummy OD, polysilicon, and metal insertion; metal over via/contact enclosure; and, redundant via insertion.

One challenge of using copper as the material for chip interconnect is that the results of manufacturing are generally different than what the designer intended. Reticle enhancement techniques (RET) such as optical proximity correction (OPC), geared to optimize minimum pitch wires, creates width variations in non-minimum pitch wires. In addition, copper is much softer than the surrounding dielectric (the insulating layer), which causes the top surfaces of the wires to wear away during the chemical mechanical

polishing (CMP) process. Processed copper interconnects have uneven copper thickness across a chip. The final thickness of a wire segment is a function of wire width, wire spacing, and metal density in that region of the chip. This results in variable interconnect sheet resistance and capacitance over the chip and, hence, variable parasitic delay, even for wires of equal length.

Ignoring the variability of copper width and thickness during chip design may result in timing simulation errors. The problem can be serious for chips 130 nm and below, particularly for faster interconnect paths. To reduce timing simulation “surprises,” intrachip metal variation modeling is key in chip design flows—Reference Flow 4.0 supports this feature. Recently, TSMC validated the Cadence Fire & Ice® QXC extractor with new-generation 3-D models to accurately account for copper and optical effects. This technology enables designers to reduce timing margins and improve the performance and yield of their designs.

Dummy metal insertion is the primary technique used to increase the uniformity of copper across a chip, thereby reducing intrachip metal variation. A key consideration in dummy metal insertion is that the inserted metal has minimal impact on signal wire resistance (due to density and RET impact) and wire capacitance (due to coupling). Therefore, timing simulation must be based on RC parasitic data that accounts for the impact of dummy fill. TSMC and Cadence have recommended design flows to insert dummy fill and account for its impact on design behavior. The NanoRoute routing solution supports dummy metal insertion within Reference Flow 4.0.

When processing chips at 130 nm and below, TSMC provides both a set of minimum design rules and a set of stricter design guidelines to enhance yield. In addition to double vias on wide metal lines, TSMC recommends a redundant via insertion methodology to enhance chip yield when there is room to add larger via structures (double vias and vias with extra metal enclosure, also known as “fat” vias). Reference Flow 4.0 recommends redundant vias on normal signal lines as well as wide metal lines, when there is room to place the extra vias, by defining a four-stage redundant via insertion flow (fat double via ->normal double via->fat single via->normal single via). The NanoRoute tool supports this methodology, with the four types of vias defined in its place-and-route technology files.

4 CUSTOMERS WIN

The collaboration between Cadence and TSMC in developing a nanometer design flow allows both companies to leverage their respective technological expertise in process development and design infrastructure, tools, methodologies, and design capabilities. The result is a higher level of silicon success, better chip yield, and substantial savings in time and money.



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