

**ANALOG DRIVEN PHYSICAL IMPLEMENTATION FLOW:  
THE ADVANCED CUSTOM DESIGN METHODOLOGY**

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## OVERVIEW

This paper describes the analog driven physical implementation flow in the Cadence® Virtuoso® custom design platform. The Virtuoso platform targets full-custom designs across the diverse design domains of analog, custom digital, RF, and memories/arrays. The platform also handles the integration of IP from these diverse domains, including importing digital standard cell blocks with an integration strategy and methodology.

The Virtuoso platform is based on an overarching methodology that addresses each design domain and subsequent integrations, and is designed to serve as a “blueprint” against which any platform targeting custom design can be measured. The advanced custom design (ACD) methodology white paper is available at [www.cadence.com/virtuoso](http://www.cadence.com/virtuoso).

The analog driven physical implementation flow is based on the ACD methodology and is one flow element of the Virtuoso platform.

## THE ADVANCED CUSTOM DESIGN METHODOLOGY

The ACD methodology is represented in Figure 1. Predictability is the driving force behind this methodology and is based on two primary concerns: 1) a schedule is met from the beginning of the design process, which necessitates a fast path to tapeout; and 2) performance requirements are met to achieve first-pass success, which requires a silicon-accurate methodology.

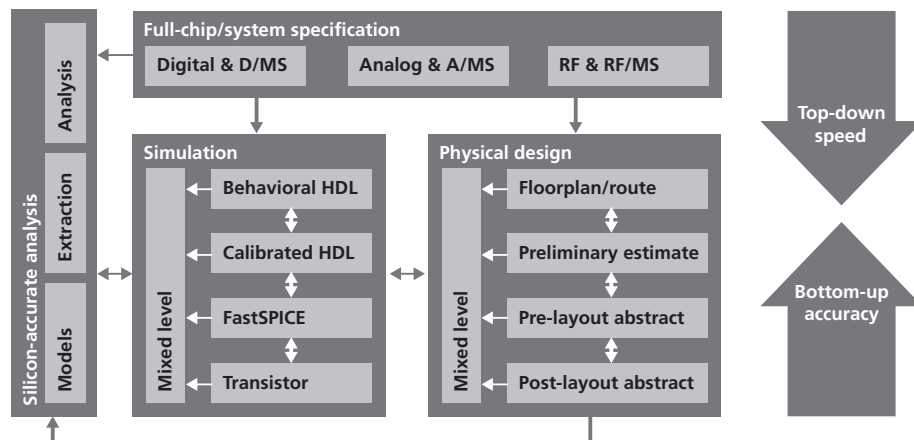


Figure 1: Advanced custom design methodology

Meeting a schedule requires a fast design process that supports thorough and complete simulation and physical design. The design process is comprised of many tasks, and many of today's chips contain multiple blocks from multiple design domains. This, it is imperative to simultaneously design in as many blocks as possible and perform as many tasks as possible, and to leverage as much of the top-level IP throughout the process as possible. This leads to the concept of design evolution, wherein all the design IP is leveraged as it matures throughout the design process. The top-down design process, when applied to both simulation and physical design, is the approach that facilitates a fast design process. Multiple abstraction levels, from high-level design through detailed transistor-level design, are combined to support a mixed-level approach that targets only the points needed for a given test. This allows designers to leverage the top level, use that information for block design, and subsequently re-verify the blocks in the top-level context.

At the other end of the spectrum is the need for silicon accuracy to achieve the required design performance. Silicon accuracy relies on the base design data, such as device models supporting accurate simulation and technology files supporting interconnect, physical verification, and analysis. Test chips, which often consist of critical structures known to be highly sensitive, are also used to verify the feasibility

of a process and the accuracy of its corresponding process design kit (PDK). Often, a design group will need to add components to the PDK to support a particular design style. Device models may need to be expanded to combine or add corners, statistical modeling, or other approaches that the design team needs.

The silicon-accuracy data is driven through the design process via detailed transistor-level analysis, which includes layout extraction. This lower level of the abstraction chain then supports the calibration of these results to higher levels of abstraction. This comprises the bottom-up design portion of the ACD methodology.

The top-down and bottom-up processes work in parallel to produce a “meet-in-the-middle” approach. It is this approach that balances the need for speed through the design process and silicon accuracy, ultimately producing a predictable schedule leading to first-pass success.

The ACD methodology can be applied to a complex integration or a particular domain area. Each domain applies the meet-in-the-middle approach, combining top-down speed with bottom-up silicon accuracy.

## THE PHYSICAL IMPLEMENTATION CHALLENGE

The Analog driven physical implementation flow accepts IP across multiple design domains to provide a physical design integration solution for mixed-signal macrocells through large mixed-signal systems-on-a-chip (SoCs). The flow encompasses floorplanning through tapeout. Its intended use is for the full-custom designer who performs integration of several blocks, whether the design itself is a block to be used in a larger, digitally dominated integration or a complete, mixed-signal SoC, for which a full-custom designer performs the integration and digital blocks are read in.

The Analog driven physical implementation flow accepts IP from the block design domains of analog, digital, and RF, and primarily performs floorplanning, routing, physical verification, and chip finishing. Any design may have a combination of integration requirements, pulling in IP from one to several domains. Figure 2 shows the full scope for a multidomain SoC.

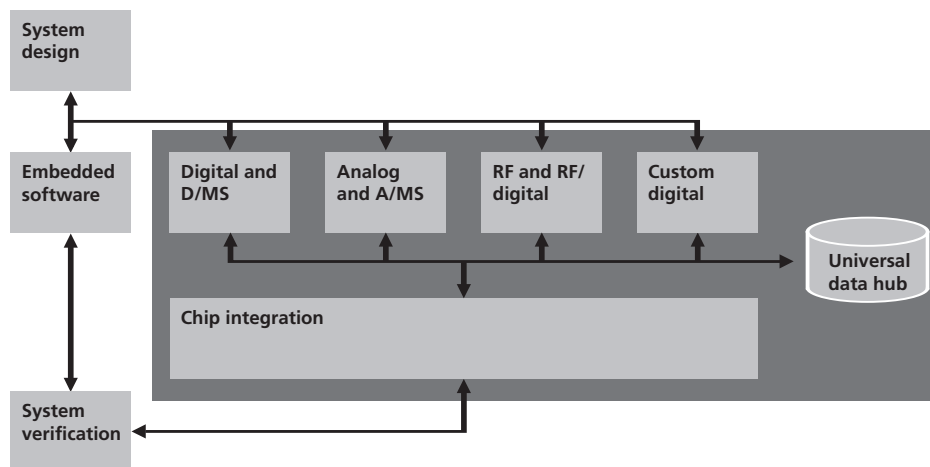


Figure 2: Multidomain integration scope

As this solution is aimed at the full-custom designer, it works in conjunction with the Cadence Encounter™ digital IC design platform, which targets the digital IC designer. This leads to two primary scenarios. The first is a full-custom designer creating a macrocell for delivery to a larger SoC. This macrocell may have digital content as well (typically around 50 K gates) along with several full-custom blocks. In this case, the Analog driven physical implementation flow would be used to create the macrocell. Since the macrocell is not a full chip, the chip finishing portion of the flow would not be needed. The finished macrocell would be delivered to the SoC team, which would read in the full-custom IP and perform chip integration using the Encounter platform. Floorplanning at the macrocell could deliver to the Encounter

platform an abstract and receive from the Encounter platform a full layout for the digital portion. Routing and physical verification would take place, delivering back to the SoC team the full macrocell.

The second scenario is a full chip consisting of several analog blocks and a small number of digital blocks, in which the digital blocks can be of varying size, but contained and not have timing dependencies at the integration level between them requiring a timing driven solution.. In this case, the design would be integrated from a custom point of view,=the digital blocks would be treated the same as in the macrocell scenario, and floorplanning would proceed at the full-chip level. When the chip is routed and physically verified, the chip finishing section of the flow would be utilized. This enables edits on extremely large databases for small last-minute tweaks, scribe lines, logos, etc. Physical verification is again performed, along with tapeout tasks such as metalfill.

Picking which solution to use, and where, is dependent on the type of design and the skill set of the team performing the integration. For large amounts of data, the OpenAccess database aids in the interoperability of custom and digital-based solutions. In general, the Analog driven physical implementation flow works best with a block-level design, with several analog blocks that may have interdependencies, and with a small number of digital blocks that are not timing interdependent. (If they are, it is better to combine them in the Encounter platform). In this case, the added ability to perform custom and analog routing in an environment familiar to the integrator is highly useful.

Another consideration is how well the flow can deal with design derivatives. In a high percentage of cases, designs are actually derivatives of previous designs, which means that using a meet-in-the-middle methodology is imperative. Some blocks will be new; many will be fixed in size and considered hard IP. This makes simultaneous support of top-down and bottom-up designs a necessity.

The physical design process is always at the end of a tight schedule and squeezed to meet tapeout schedules. To meet this challenge, the full-chip assembly and verification process must be highly predictable, especially in the final weeks before tapeout. This is not the time to find routing or verification issues. As a result, the best approach is to rely on continuous evolution, wherein the design is built continuously as new block configurations are passed to it. Continuous evolution is to physical design as continuous regression simulations are to simulation and verification. This approach is the key to meeting a schedule. When executed, last minute changes are effectively added to a known process, ensuring a predictable design schedule. Problems are caught early on during the first several builds, when there is time to deal with them.

Another key output of the physical design process is parasitic information. From a physical design process perspective, parasitics are not used; however, front-end simulation teams rely on parasitic information. Thus, it is highly useful for top-level route parasitic information to be gathered and passed to block designers early in the design process. This allows block-level designers to use the information as block-output loading specifications. Critical nets can be identified and continuously checked, early and often.

In addition to parasitics, silicon analysis can be performed early in the design process or as part of the continuous evolution capability.

Thus, a successful analog driven physical implementation flow contains:

- The capability to bi-directionally pass data between multiple design domains
- Floorplanning capability to facilitate top-down and bottom-up design, early on
- Analog routing capability to facilitate continuous evolution
- Parasitic and analysis capability, early and often
- Chip finishing capability for large design databases

## THE ANALOG-DRIVEN PHYSICAL IMPLEMENTATION FLOW

The Analog driven physical implementation flow must accept design collateral from multiple points. Digital content is expected to enter the flow from being created within a digital environment and thus the two environments are required to interoperate. The flow is represented in Figure 3.

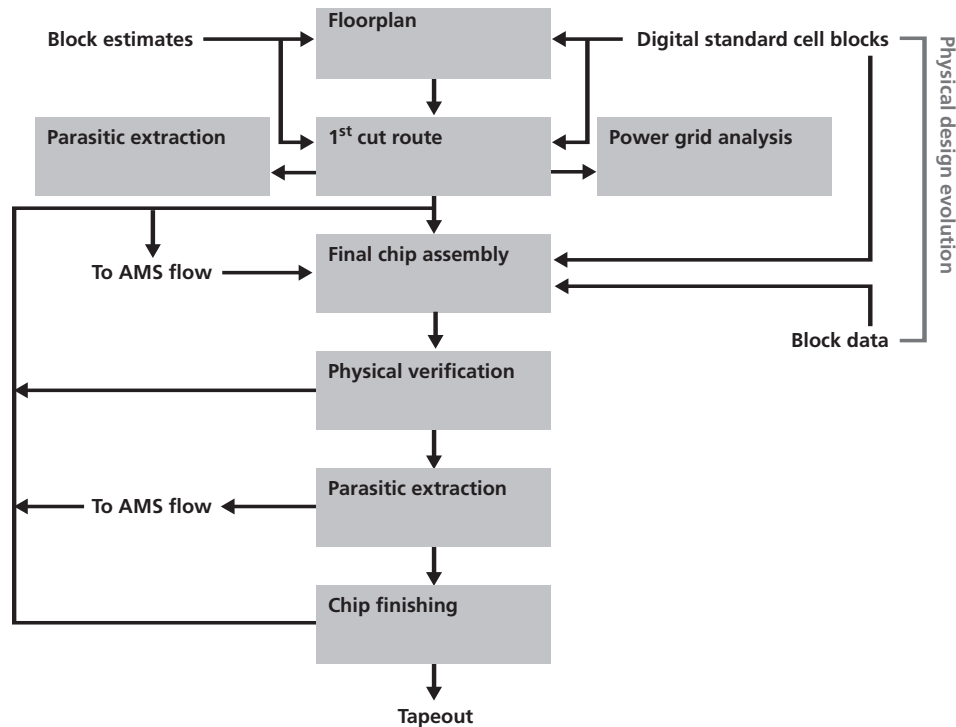


Figure 3: Analog-driven physical implementation flow

The floorplanning stage can accept abstracts based on a variety of input, whether they are completed hard IP or area estimates from partially completed designs. Here the designer has the ability to make tradeoffs on those design pieces that can change, and optimize placement and pin locations for routing. Abstracts for “soft blocks” (those blocks that will be redesigned and therefore are able to be modified) are passed back to either the block creation flow (part of the Virtuoso AMS flow) or to the Encounter platform (for digital content).

With a completed floorplan, blocks start the design process and a first-cut route can be performed. This gives designers early information on how routable the design is, and the floorplan can be tweaked accordingly. Scripts are set up to enable as repeatable a process as possible—the more repeatable subsequent iterations are, the more likely they will be run. The designer should also capture any design IP or knowledge (i.e. critical nets that are routed manually, areas to watch out for) in case others need to run the design through the flow.

With an initial route in place, the designer can generate parasitics for the top-level nets (either all of them or critical nets that are identified). Early on in the design process, this serves as block-level specifications and loading characteristics, which are used for the simulation process (discussed in the Virtuoso AMS top level reference flow whitepaper, available at [www.cadence.com/virtuoso](http://www.cadence.com/virtuoso)). This is critical to ensure fewer iterations in block-level design and smoother top-level simulations, producing fewer surprises at the end of the design cycle.

As blocks mature, repeated iterations are performed at the top level, enabling a continuous evolution methodology. This process continues until all blocks are considered final, whereupon a final route is completed.

Physical verification is performed at each routing stage. As blocks become final, they are “mastered” into the database and re-verified in the top-level context. At final verification, the full database exists with all block-level representations. At this point, final RCX runs are produced (and again passed to the AMS flow for verification purposes).

Chip finishing allows for the final edits necessary to make the database tapeout ready. These tasks run on the full database and, often, large digital content makes this a large entity. In some cases, design tweaks (perhaps metal changes) may be necessary at this level. Before tapeout, tasks such as adding scribe lines and logos necessitate access to the full-chip-level database. Finally, tasks such as metalfill or other foundry-specific requirements must be performed, after which tapeout can occur.

The combination of Virtuoso platform tools (such as the Preview option, Virtuoso XL, the Virtuoso Chip Assembly Router, the Assura™ DRC/LVS/RCX verification suite, ) enables such a flow to work.

## **CONCLUSION**

The Analog driven physical implementation flow is a key element within the Virtuoso platform, enabling full-scale integration across multiple design domains from a full-custom point of view. The versatility in its interaction with other solutions, such as the Encounter platform, enables the right solution to be applied to the right design task. The Analog driven physical implementation flow can be used from macrocell development through full, mixed-signal chip integration.



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