

**ANALOG BLOCK CREATION FLOW WITH
REUSE AND MIGRATION REFERENCE FLOW**

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OVERVIEW

Creating AMS and analog IP is traditionally more an artform than a repeatable process. Yet today's complex ICs, and the ever increasing need for efficiency due to a shortage of analog engineers and tight design schedules, makes it paramount for analog engineers to design their IP to allow for others to at least leverage from it and ideally reuse as much as possible.

The concept of any form of reuse in analog design has largely been rejected, due to the nature of analog itself — highly sensitive to process variations, noise, circuit topology and other design issues which leads to the assumption that analog circuitry must always be redesigned. This often puts the analog and AMS pieces of a complex SOC on the critical path to tapeout. These concerns are real and no potential solution to the problem can overcome the laws of physics.

However, the creation of any analog block involves the creation of a number of layers of “design collateral” such as models, testbenches, simulation setups and results, etc which at the very least have the potential to be reused for the next design variation. This leads to the concept of leverage — rather than full reuse — that is the next designer can leverage off of the existing design database for reusable pieces of the design. With a repeatable block creation flow, another designer can analyze an existing design and determine what pieces may be reusable for the task at hand. After this determination, depending on the design task, it may be possible to leverage the design itself to either tweak to a new specification or even migrate to a new process through increased use of automation.

A REPEATABLE PROCESS

Any chance of reuse or even leverage starts with the initial creation of the block in question. Analog designers are notoriously skeptical of anything they themselves have not designed, therefore to allow for any leverage from an existing piece of IP, the “new” designer needs to gain confidence in the existing design and gain a thorough understanding of it. Second, if this piece of IP is to be used anywhere else, the block creation flow must output the appropriate collateral for both an initial determination of applicability and subsequently an exhaustive reverification of the design itself for use within a new SOC. Figure 1 shows a flow that can be used for this purpose.

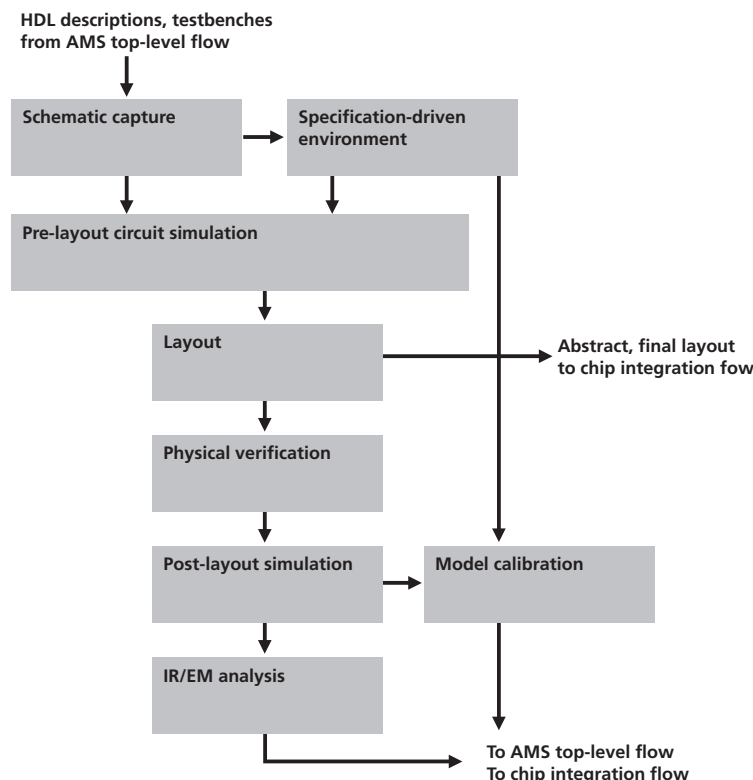


Figure 1: Initial block creation flow

It should also be noted that for any reuse to occur, the design collateral that supports reuse and repeatability needs to naturally fall out of the design process. If supporting reuse/repeatability requires a significant overhead, it is unlikely to occur. Therefore, the initial block creation flow provides a method for block creation where design collateral is used during the initial creation process and for the integration flows, meaning that this design collateral is a natural fallout of the design process. At the end of the project, it is not expected to have a “reuse task” where the designer is expected to produce the extra collateral necessary to support potential reuse down the road. This is then tied into top level simulation and physical integration flows that effectively use the design collateral produced.

The central element to this flow is its link to the top level integration flows for simulation and physical implementation. Initially, if this block is going to be considered for use in another design, a high level behavior model and a bottom-up calibrated model would be highly useful for this exploration phase. The high level behavioral model supports the initial top down simulation process at chip level, where the block can be analyzed for its applicability in a new design. The bottom-up calibrated model contains actual simulation parameters from transistor level simulation to provide a more accurate model which mimics the performance of the block. This is useful if the block will be reused in a design on the same process technology node that it is currently designed with. Abstracts and layout data also need to be easily accessible for initial floorplanning and physical integration work.

Under the assumption that the block has potential to be leveraged, it is imperative that the complete suite of simulations exist in a repeatable form. This allows the new designer to understand the specifications and tests the block was designed to, and verify that all simulations can be rerun and results are consistent with the original design. This is best accomplished through a specification driven environment, where all specifications and results are captured in a repeatable form, complete with datasheet creation — where the designer can match the resimulations to the original results. Only through this reverification process will the new designer gain confidence in the design, and it also quickly allows him/her to gain familiarity with the design itself. For example, even if the block is to be reused on the same process node, it might need to be reverified due to device model changes in a process update or a number of other reasons. Simulations could be run using either a fastspice simulator or a traditional spice level simulator. Any new tests that are necessary but weren't included in the original design can be added.

All setups to run key steps such as DRC and LVS, as well as parasitic extraction, are necessary to be repeatable as well. Process updates may also tweak parasitic technology files which require a full postlayout reverification. This requires either notes on the schematic or separate documentation describing any critical portions to the circuit that are necessary, such as matched pairs, differential routes, etc. This is important to allow for any new tweaks that may be needed to the block for its new intended use.

Connectivity based layout helps in this as well — allowing for a new designer to pull up the schematic and layout and make modifications or explore the design more easily. Any steps through the layout process that take advantage of capabilities like automated placement or routing should be repeatable as well to facilitate any layout changes in an expedited manner.

Analysis capability such as IR drop and electromigration need to be run for use in top level analysis. As such, these runs need to characterize the block level performance — and if necessary be rerun to ensure the integrity of the top level analysis.

The composite total of all the setup files, results, and information form the design collateral for the block. It is this design collateral that captures the designer intent or “designer IP” that in all cases can be leveraged. With this repeatable process and accessible design collateral, it can be quickly determined the feasibility of leveraging or reusing the block in question.

MIGRATION OPTIONS

Let us now assume that the design challenge involves more certain modification to the original design or perhaps migrating the design to a new process. This is where usually an analog designer will claim the circuit needs to be redesigned due to the challenges mentioned above. This may be the case, however there exists two potential options by which more reuse or leverage could occur. This involves two parallel paths, one leveraging off the existing layout data, the other leveraging a more automated rapid analog design methodology. Figure 2 adds to the block creation flow with these two paths.

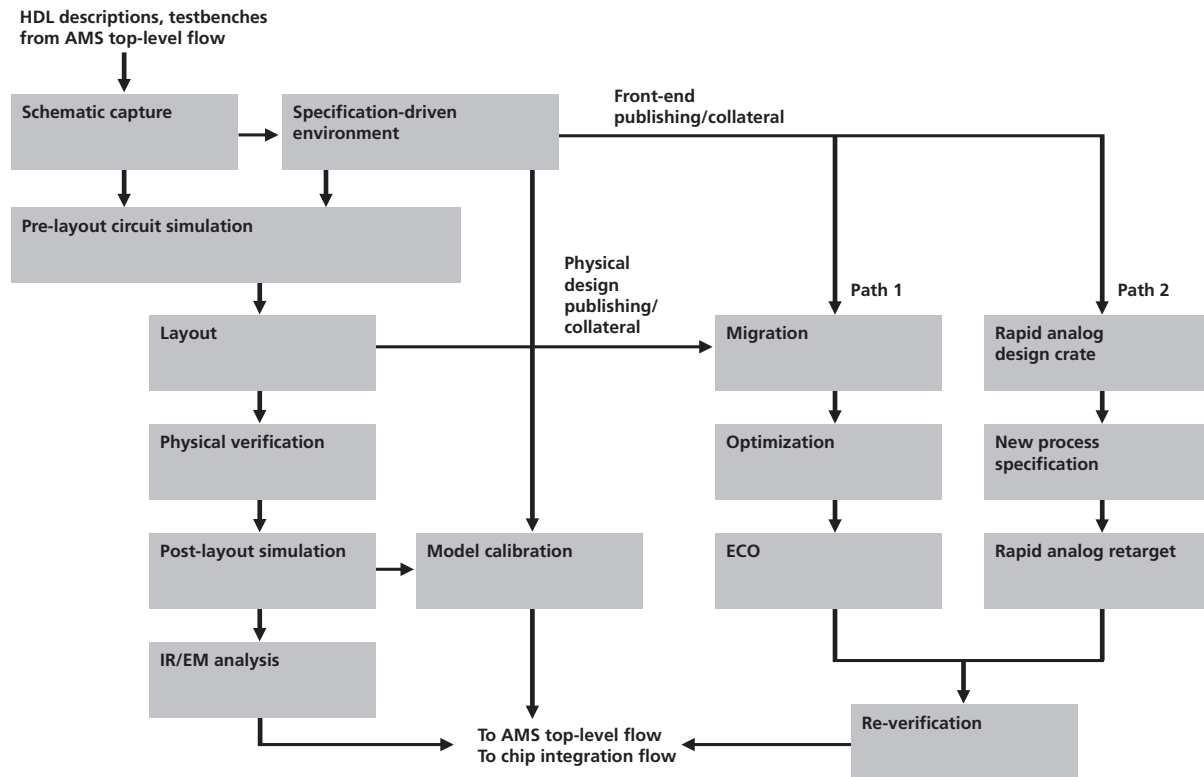


Figure 2: Analog Block Creation with Reuse/Migration

First we shall consider "Path 1". In this case, we have an existing layout database that we may believe we could use automation to migrate to another process. Our expectations here are not for a 100% scalable outcome, however we can take advantage of automation that can migrate the schematic and the layout to the new process by using mapping rules specified between the two process nodes. At this point, we have a design database at the new process node which meets design rules. It may or may not however meet design specifications.

Our repeatable regression suite can be applied to initially test the block that has been recently migrated. Based on these results, let's assume that the block doesn't quite meet the design specifications after the initial migration. At this point, parasitics can be extracted and the circuit can be optimized using automated transistor sizing based on target specifications. This is in fact now modifying the design, however in a constrained way. We can now capture the ECOs and feed these back into our migration tool to allow automation to help update the layout based on the new sizing we have from the optimization tool. Finally, the block is reverified against the full regression suite once again. In this way, the initial design is leveraged as much as possible. This approach can work if the block is conducive to the initial migration where it is close enough that specifications can be closed through the use of automated sizing, and not require major overhauls to the design.

Another option to consider is "Path 2". In this case, let's assume that either we are willing to largely redesign the block, or that we feel the layout migration path incurs too much risk. A rapid analog design capability can be employed which first can create an analog block by leveraging automation in transistor sizing and layout creation, and then allows for a repeatable migration scenario by leveraging the topologies and setups from the original design. The constraint here is the block must be initially created using this rapid analog design capability.

An initial topology is provided, along with design specifications (consistent with the repeatable regression suite described above), parameterizations, and physical constraints. This approach leverages automation to automatically optimize the circuit design to meet specification and subsequently create the layout based on the topologies provided. All of these topologies and specifications then are leveragable as the design is then retargeted, and the repeatability requirement is also met through a more automated approach. In effect, the designer starts over by leveraging the same topologies, updates the design specifications, and then recreates the design in the new process node using the rapid analog design capability. The other elements of the creation flow are then applied such as IR/EM and any additional tests necessary, behavioral models created, etc.

CONCLUSION

Creating and reusing or leveraging analog blocks is a controversial subject, yet with more advanced approaches achievable nonetheless. The basis is a repeatable initial creation process whether the block is created in a traditional manual approach or with a more automated approach. Design collateral central to any reuse possibilities is generated as a natural fallout of the design process, reducing or eliminating overhead after tapeout. Migration, while tougher to automate, can be aided through the use of a layout migration based methodology or through a more automated rapid analog design approach. These gain the most leverage from the existing design and also save significant schedule from a manual approach.



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