WHITE PAPER

AMS TOP LEVEL FLOW

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OVERVIEW

This document describes the AMS Top Level Flow to the Cadence Virtuoso Custom Design Platform. The Virtuoso Custom Design Platform targets full custom designs across the diverse design domains of analog, custom digital, RF, and memories/arrays. The platform also deals with integrating IP from these diverse domains, including importing digital standard cell blocks with an integration strategy and methodology.

The platform is based on a overarching methodology with deals with each design domain and subsequent integrations, and is designed to serve as a "blueprint" to which any platform targeting custom design can be measured. The Advanced Custom Design Methodology (ACD) document is available at cadence.com.

The AMS Top Level Flow is based on the ACD Methodology, and is one flow element of the Virtuoso Custom Platform. Its scope is defined as top level simulation in and analysis, and works closely with the AMS Block Creation Flow and Analog Driven Physical Implementation Flow (information available at cadence.com).

THE ADVANCED CUSTOM DESIGN METHODOLOGY

The methodology is pictorially represented in figure 1. Predictability is the driving force behind the ACD methodology. Predictability is predicated on two primary concerns: schedule is met from the beginning of the design process necessitating a fast path to tapeout, and performance requirements are met to achieve first pass success — requiring a silicon accurate methodology.

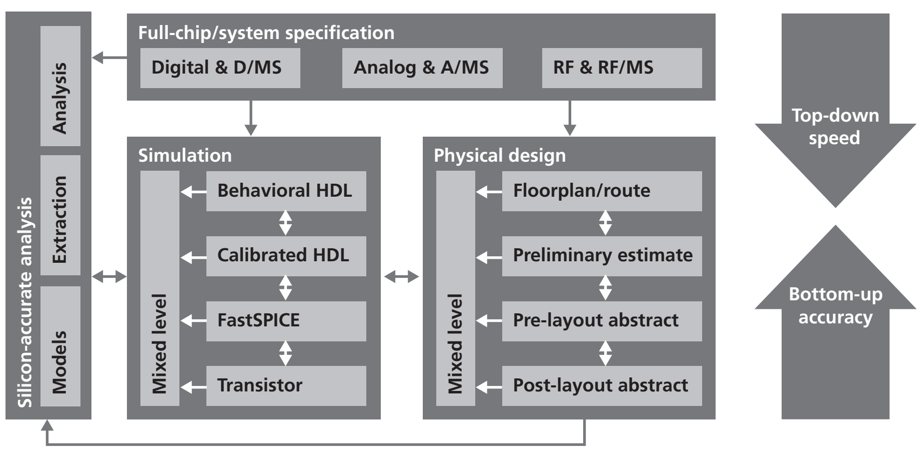

Figure 1: Advanced Custom Design Methodology

Meeting schedule requires a fast design process which supports thorough and complete simulation and physical design. The design process is comprised of many tasks, and many of today's chips contain multiple blocks from multiple design domains. Thus, it is imperative to design in as many of these blocks and perform as many tasks as possible in parallel, leveraging as much of the top level IP throughout the process as possible. This leads to the concept of design evolution, where all the design IP is leveraged as it matures through the design process. The top down design process when applied to both simulation and physical design is the approach that facilitates a fast design process.

Multiple abstraction levels, from high level design through detailed transistor level, are combined to support a mixed level approach which targets detailed design to only the points needed for a given test. This also allows for leveraging the top level and using information from that for block design, and subsequently re-verifying the blocks in the top level context.

At the other end of the spectrum is the need for silicon accuracy to achieve the required design performance. Silicon accuracy relies on the base design data such as device models supporting accurate simulation, and technology files supporting interconnect, physical verification and analysis. Test chips, which often comprise of critical structures known in the past to be highly sensitive, are also used in this process to verify the feasibility of a process and the accuracy of its corresponding process design kit (PDK). Often times, a design group will need to add additional components to the PDK to support a particular design style. Device models may need to be expanded upon to either combine or add corners, statistical modeling, or other approaches the design team needs.

The silicon accuracy data is driven through the design process through detailed transistor level analysis, including layout extraction. These comprise the lower level of the abstraction chain, which then support the calibration of these results to higher levels of abstraction. This comprises the bottom up design portion of the advanced custom methodology.

The top down and bottom up processes work in parallel producing a "meet in the middle" approach. It is this meet in the middle approach which balances the need for speed through the design process and silicon accuracy, ultimately producing a predictable schedule leading to first pass success.

The Advanced Custom Design Methodology can be applied to a complex integration or a particular domain area. Each domain applies the meet in the middle approach, combining top down speed with bottom up silicon accuracy.

THE AMS DOMAIN

An overall design process consists of processes targeted to a particular design class and thus a particular user base. For any tool to be used effectively, it must be a natural part of the environment a particular engineer is using. At integration (ie when analog, digital, and RF are brought together), special attention needs to be paid to who will be running the top level simulations and performing top level physical design, and where design collateral (netlists, databases, etc) is coming from. It is helpful to take a similar approach to designing this "design system" as an SOC designer would take on his chip.

Figure 2 shows the scope of a complex system comprising several design domains. Each box on this diagram can be considered a "block of the chip," where requirements exist within the "block," and "block IO" requirements exist to support integration. The end simulation system must support full mixed signal capability from both a custom point of view and a digital point of view. Each "block" produces design collateral (netlists, models, simulation setups, etc.) which must be 100% compatible for integration from either the custom or digital point of view.

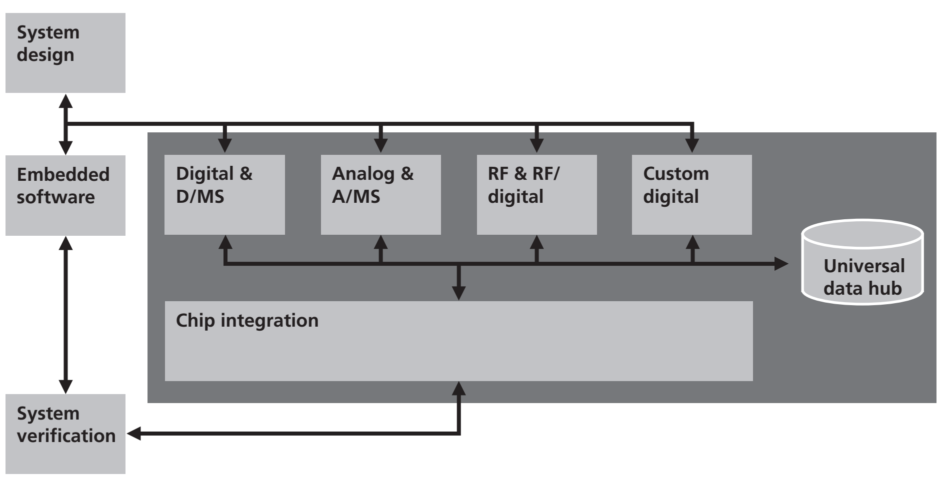

Figure 2: Multi-domain Integration Scope

The AMS domain, as defined for this document, consists of analog simulation at the top level. Other AMS based flows that interact with the top level flow include the AMS block creation flow and the analog driven physical implementation flow (which can be accessed through cadence.com). AMS also consists of simulation including digital content (imported from the digital domain) for mixed signal simulation.

Looking at the problem top down, for integration to be realized the designer is responsible for the proper design collateral existing and ready to use as is. In the design world there is a "design chain," where suppliers feed primitives to IP groups, who design IP blocks which are fed to design groups, who then integrate and design other blocks to produce the chip. Any link that is broken in this chain causes the system to break down. Similarly, there is a "collateral chain" within the design process, targeted to design collateral which will be used at the next integration level. Figure 3 describes an example of this chain relating to behavioral models for design blocks.

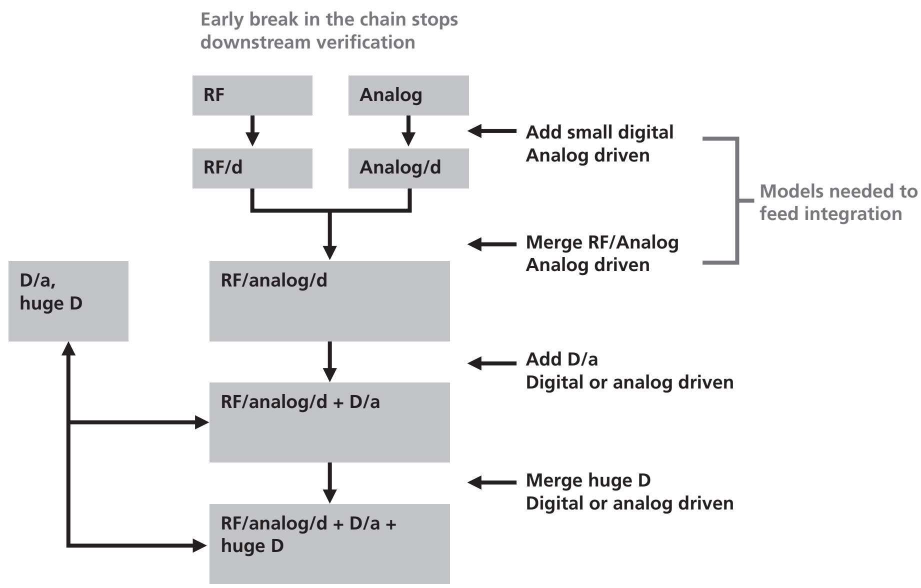

Figure 3: Collateral Chain Supporting Integration, Custom Point of View

From the custom point of view, circuit blocks are designed, and then blocks are brought in for integration. The design focus is either on the circuit block in the case of the design task, or measurements driven from or dependent on the custom blocks at the verification task. To achieve the final level of integration, all previous steps must be successful. Jumping from "Analog" at the top to "RF/Analog/d + D/a" near the bottom would unlikely produce a successful outcome. A top level simulation strategy, based on a multimode simulation capability, defines what collateral is needed for each integration level, the design tasks for each circuit block/designer and the verification needs for that collateral. The incremental approach ensures that each piece of the puzzle can fit together in a phased approach. The same simulation can be run from either the digital or custom point of view where appropriate. A similar picture can be drawn from the digital point of view, where analog collateral is referenced as integration progresses. The effective integration of this design collateral supports a fast design process.

To effectively use this multimode simulation capability, it is imperative the design team devise a simulation strategy prior to design start, specifiying what levels of abstraction to use for what simulations. This needs to encompass top level and block level — block level may be a transistor level within a top level context at HDL, top level may be fully HDL or FastSPICE level. This then is used to ensure all abstraction levels are created to support the simulation plan.

Multiple power supplies are a common characteristic of mixed signal designs. The ability to manage these in an effective manner, without having to specifically maintain separate versions of each block depending on which supply is being used — with smooth follow through from simulation through LVS — greatly aids the design process.

Analog design is also highly dependent on silicon effects, requiring a silicon accurate capability and bottom up flow to support accurate simulation and analysis. Silicon effects, such as IR drop and electromigration, are key issues for analog designers both at block and chip level. Parasitics must also be used effectively at all levels of the design, block through chip. This bottom up capability supports the ACD methodology by capturing silicon effects, and abstracting silicon accurate simulation data into higher levels of abstraction to support a fast design process.

To meet these challenges, the AMS flow must contain:

- A specification driven environment, with the ability to capture designer IP and support continuous design evolution
- Multimode simulation, with the ability to apply and mix simulation capabilities to specific pieces of the design
- Ability to manage multiple power supplies
- Silicon analysis, to support the silicon accuracy requirements
- Process design kits (PDKs) which support the full capabilities of the AMS flow

THE AMS TOP LEVEL FLOW

The AMS Top Level Flow must support block level analog design, and then the subsequent integration of digital content. It must accept collateral from the digital domain for use from a custom point of view, as well as produce collateral for use within the digital domain. The flow is represented in Figure 4.

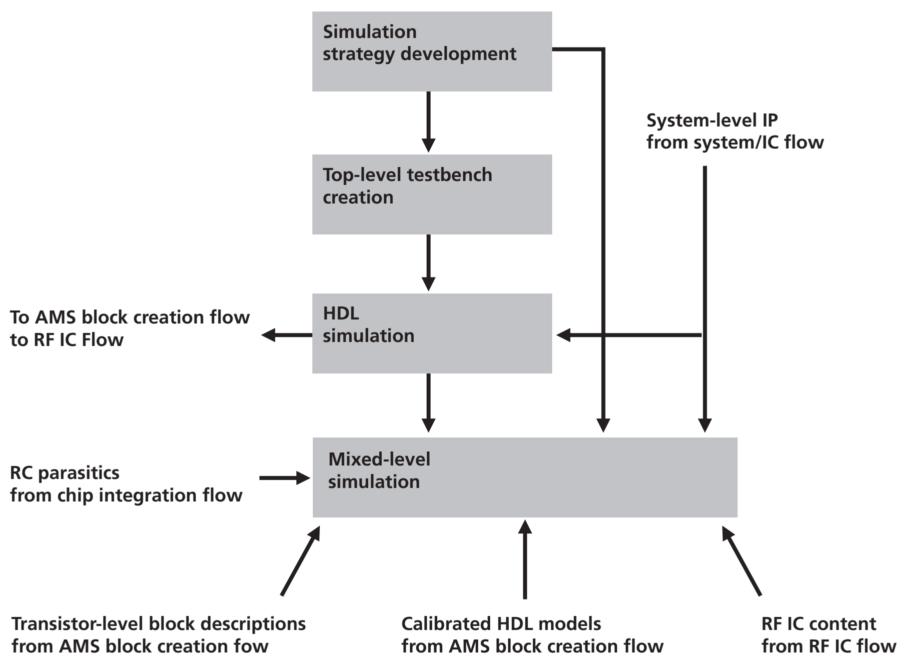

Figure 4: AMS Top Level Flow

In large analog blocks, consisting of many analog components, simulation is long and tedious. Often times a full simulation of an analog front end can't complete and doesn't get run. To facilitate this, the analog HDL models from the top level can be used as a starting point, along with the testbench setups. The first step is to take this HDL model, and partition the analog section into the next level of hierarchy at the HDL level. Similar to the top level, a mixed level plan is developed to simulate the entire analog front end. Transistor level design then can occur for each sub-block and verified both within the analog front end and at full chip level. It is often the case that multiple analog blocks will need to be simulated at device level at the same time when closed loop interaction between those blocks occur, so the analog section simulation plan must account for this.

Traditionally, SPICE class simulators have been the simulator of choice for analog designs. Because of the extreme sensitivity of many analog circuits, analog designers believe high silicon accuracy even at the expense of simulation speed is paramount, and find it difficult to trust other simulators. Yet, the speed and capacity of FastSPICE simulators, especially the ability to backannotate parasitics, is alluring. Since it is impossible to run a huge amount of devices in SPICE, it becomes a worthy tradeoff to then run a FastSPICE simulator on these leaf cells and ensure proper functionality, with perhaps some compromise on accuracy. When running large simulations, FastSPICE can often be used as a verification tool for the analog section. When combined with HDL representations, this multimode simulation capability can support a wide range of simulation options.

In parallel, transistor level results can be backannotated into analog HDL models to produce calibrated HDL models. These models will not capture all the silicon accuracy effects that can be found in transistor level, but postlayout results can be captured (whether these results come from SPICE or FastSPICE doesn't matter) producing a much more accurate HDL simulation at very fast simulation speeds. This also enhances the mixed level options, as no matter what transistor level simulator is being used, especially when accounting for parasitics these simulations are hard to set up and take a significant amount of time to run. The advantage of capturing the results in HDL is especially paramount at top level when simulating with large amounts of digital logic, aiding simulation speed. It is important to have an HDL option to the mixed level arsenal, and it benefits the analog designer natively.

With a fast analog simulation process, built on a multimode simulation capability and a thought out simulation plan, digital content represented in HDL can be added painlessly to complete the mixed signal picture.

With many corners to manage, and multiple design results to verify, simulation management is a huge issue to the analog designer. Full repeatable regression suites are necessary, which produce and document results for use in reviews or for annotation to HDL. Abstraction levels supported are fed continuously to the top level, as top level simulations are run with more and more design data annotated. Regression setups and execution are performed through the specification driven environment.

The AMS flow is based on a fully compliant PDK which provides the infrastructure for the complete process. The design team should pre-qualify the PDK before design start to ensure the PDK meets the specifications, and take action to get the PDK to standard in time to support each required design step.

SIMULATION STRATEGY

The most important step in a mixed-signal verification process is developing a top-level simulation plan, to take full advantage of the capabilities available through the Virtuoso Platform. The top-level simulation plan spells out, per simulation run/test bench, the mixed level configurations that will be used. Let's take a specific example — we will develop a simulation plan for one top-level test of a mixed signal design.

We are making the following assumptions:

- We have digital RTL from our digital design team. The RTL block will map to gate level digital standard cells during logic synthesis.
- We are starting with a full behavioral level simulation, as the blocks have yet to be designed at this stage. These results will be used for comparison as much more accurate results are obtained from the bottom up process.
- We will swap in the transistor level descriptions for one block, say an ADC. The ADC is the first block in which we get transistor level schematics.
- Our block designers are using the Virtuoso AMS Block Creation Flow, and thus we are delivered design collateral from this flow to be used to exercise the simulation plan. We will run full analog transistors plus Digital behavioral verification

- We have critical interfaces issues between two blocks. Our physical design group is using the Analog Driven Physical Implementation Flow and therefore has a first cut of top-level route. This allows us to use top-level parasitics between these two blocks as part of our simulation plan. We can verify the top-level parasitics between these two transistor level blocks with the rest of blocks in behavior/transistors level.
- Our block level designers eventually will have done all the transistors level implementation for all analog blocks, so that we can verify all analog transistors level design under the top-level test bench.
- The full parasitics simulation on all analog transistors is somewhat costly in simulation time. We will consider the analog transistors level plus digital behavior plus top-level parasitics as a "final" verification for this reason.

With the scenario outlined above, we can determine a set of configurations to facilitate the verification of this test continuously throughout the design process.

Our first simulation will be the top-level behavioral simulation. Here, each block is described in high-level behavioral form to verify the design at the architectural level.

Second, our high level behavior is partitioned into the low level behavior. The ports, cell names and hierarchy name exactly match the block level schematics to be implemented. This will be delivered as detail specifications and required result for each of the blocks to the block design team.

Third, we use the calibrated model for a performance critical block such as the PLL. The calibrated model can be created based on the schematic or extracted layout. It is provided by the characterization team by using the AMS Block Creation Flow. The calibrated model provides increased simulation speed with some transistor level accuracy.

Fourth, our adc_top transistor level block from our block design group is available. We need to verify this transistor level block in the top-level context, with the rest of the design described as behavior.

Fifth, the top_common and anlg_cntl blocks are provided from our block design group; this is our scenario where these two blocks have interface issues that need to be verified. We will get the top-level parasitics between these blocks based on the first cut of top-level routing, which has been implemented by our layout group, so that we could simulate these two transistor level blocks with early top-level parasitics under the top-level context. This allows us to use these parasitics before all the other blocks are completed at transistor level.

The fifth simulation occurs when the block design team completes the entire transistor level schematic. We want to verify the whole transistors level design with the digital behavior in top-level context.

Finally, the top-level layout routing is implemented and checked to be LVS clean. We wish to verify the full transistor schematic with digital behavior and top-level RC parasitics.

The table below summarizes our approach:

Simulation plan name	Test bench	DUT (Design Under Test)
High level behavior	RTL Verilog	High level behavior verilogams
Low level behavior	RTL Verilog	Low level behavior verilogams
Mixed behavior and calibrated model	RTL Verilog	Behavior model + PLL calibrated table model
Mixed behavior and transistors	RTL Verilog	Behavior model + top ADC transistor level schematic/netlist
Top level critical nets	RTL Verilog	Behavior model + top_common and anlg_cntl transistor level + interconnect RC between these two block
Full analog transistor	RTL Verilog	Full transistor schematic/SPICE netlist
Top level parasitics	RTL Verilog	Transistor level schematic + top-level parasitics + DSP behavior core

Table 1: Simulation Plan

SUMMARY

The AMS top level flow is a key domain within custom design, yet is not the only flow of concern. As a result, it must address the specific needs to analog and mixed signal designers, and also support integration and interoperability across other design domains. It is key to follow a coherent methodology to ensure all requirements are met. A design team should plan up front a simulation strategy, audit the PDK and silicon accuracy capabilities, and subsequently execute to plan.

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