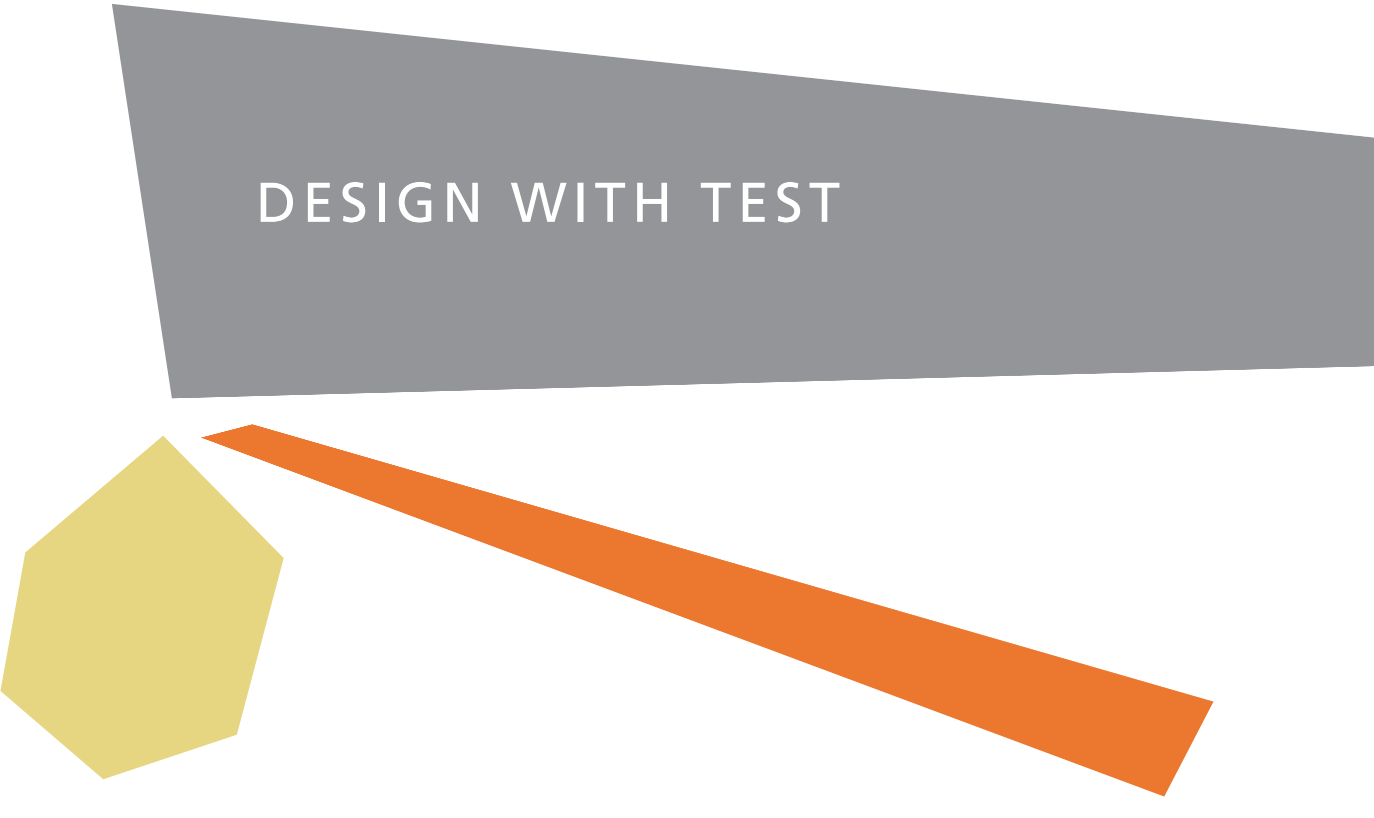
WHITE PAPER



DESIGN WITH TEST

BACKGROUND

As process geometries shrink to 65nm and below, manufacturing test must expand its role in the design, implementation and production of semiconductor devices. Much like DFM and its manufacturing-driven design flow, which is an accepted requirement today, a "test-driven" design and implementation flow is now at the forefront of chip design concerns. The key drivers for this change include: the need for delay test to ensure product quality, the requirement for on-chip test data compression to reduce the cost of test, the significant growth in the use of on-chip memory blocks, the wide adoption of low-power design flows, the increased power consumption during test, and dynamic defect behavior caused by advanced physics effects in nanometer technologies. These factors contribute to a highly complex interaction among test and the design and implementation flows. As this emerging role for test is broader than traditional Design For Test (DFT), we refer to it as "Design with Test".

DFT methods in use today are no longer sufficient for sub-nanometer devices, since they are limited to integration at the level of interoperability among different tools in the design and implementation flows. In order to address the complexity of 65nm designs and the challenges of timely design closure, test must be fully integrated up front in the design process by modeling its interaction and interdependence with synthesis, floorplanning and placement/routing. A Design with Test approach enables this through "a deep level of integration" with these design steps.This integration is essential to model complex interactions accurately while generating the highest quality of silicon.

METHODOLOGY REQUIREMENTS

Structural test methods are used to validate that every semiconductor device has been processed in the fab without any manufacturing defects. In nanometer process technologies, delay tests using timing-aware Automatic Test Pattern Generation (ATPG) engines that target the transition fault model are required to detect the predominant delay defects found in sub 90nm devices.

ATPG for the transition fault model is a key example of the need for deep integration of test pattern generation with design timing. Recent empirical studies using a statistical quality defect model proposed by STARC—the Semiconductor Technology and Research Consortia, which is composed of eleven Japanese semiconductor companies—presented at ITC-2005 supported this need. These studies demonstrated conclusively that transition tests that use actual circuit timings to create tests with the tightest possible timing detect a greater number of small delay defects, providing up to 40% improvement in the dpm (defects per million) metric. This directly translates to the business challenge faced by semiconductor manufacturers of meeting the stringent requirements of shipped product quality levels—a requirement that is hard to meet without the test-timing integration, making Timing-Aware ATPG a must-have technology.

In addition to inserting scan chains to support Timing-Aware ATPG, there are several other test-specific on-chip structures that are required to achieve the desired results in terms of test coverage and lowered test costs. These include boundary scan to enable structural board-level test, memory built-in self-test (BIST) to test embedded memory, on-chip test data compression to reduce test volume and ATE time, on product clock generation to support transition testing, IEEE 1500 core test to support SoC test methods, etc.

All of this required test structure insertion activity must be completed before timing closure can begin. Once in timing closure, any changes to the design hierarchy or placement can cause additional re-spins of the test step.

On-chip Test compression in particular has a direct bearing on the device cost. The insertion of on-chip compression logic to manage test cost results in a small number of large scan chains being fragmented into a large number of small scan chains. To alleviate these challenges, the insertion of test structures such as compression must take physical constraints into account—again enabled by the "deep integration" with the design flow—in order to fully realize the cost benefits of compression.

These same considerations of on-chip compression also hold for other test structures such as Memory BIST and uncompressed scan chains. In particular, the need to share Memory BIST engines among multiple memories requires a concurrent optimization of placement and DFT insertion to optimize their proximity in today's complex SOCs, which contain a large number of discrete RAMs/ROMs.

Verification and test also have strong linkages that ensure the tests run the first time on the tester with highest coverage. To meet aggressive design schedules Test Generation must be correct the first time as defined by test programs that run on Automatic Test Equipment (ATE). Customers cannot afford test debug test patters during the manufacturing ramp of the product. Test features that are inserted in the design need to be validated with the same rigor as non-test functional features. The best way to guarantee that tests will turn on the first time at the tester is to have a robust verification and simulation of the test features prior to chip tapeout. The Design with Test approach holds the potential of reducing silicon iterations and enabling a reduction in time-to-volume production.

With the concern over power consumption moving from being a functional mode only concern to other modes of operation including test, the interplay of test with the implementation flow takes on special significance. Excessive power consumption in the test mode can result in false fails or even destruction of the device under test unless the test patterns are constructed with a full understanding of the power structure and the device's power consumption limits. Patterns that are typically constructed for test have traditionally tended to ignore power consumption in that their objective was to maximize the fault coverage for each pattern regardless of switching activity, reducing the number of patterns to be applied and thereby reducing the time on the tester. Further sensitivity to the power constraints for a given device can be realized by recognizing the power management techniques incorporated in the device by the designer.

This brings us to the last example demonstrating the increasing need for "deep integration and design with test" extending beyond the design domain into the manufacturing yield domain. With the advent of nanometer technologies, design yields are more limited by design content "features" than by random defects. In order to bridge the gap between feature-limited and defect-limited yield, diagnostics based yield ramp and yield learning technologies are becoming deeply integrated into the design flows to impact the yield ramp.

CONCLUSION, RECOMMENDATIONS

The quality, cost, and yield challenges in nanometer test represent a unique opportunity for the EDA industry to provide higher value and become a trusted advisor and partner to its customers. Semiconductor manufacturers can expect Design with Test methodology enabled by a tight integration of test in the design and implementation flow to reduce silicon iterations and realize reductions in time-to-volume production. A key enabler for such holistic solutions is a deep level of integration of all aspects of Test (DFT, timing-aware ATPG, and yield diagnostics) in the design, implementation and manufacturing flows.

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