WHITE PAPER

MODEL-BASED METHODS CRITICAL FOR EFFECTIVE MANUFACTURING-AWARE PHYSICAL DESIGN

BOB NABER AND NITIN DEO

cadence™

INTRODUCTION

As semiconductor companies move to more advanced technology nodes, integrated circuit (IC) design teams find more manufacturing effects exerting a larger impact on silicon performance and yield. Designers using traditional methods continue to face significant challenges in reliably meeting yield and performance objectives for current technologies–and will encounter more serious limitations at next-generation technology nodes. New approaches based on flexible, accurate modeling methods allow engineers to exploit manufacturing knowledge early in the design flow to avoid yield problems while fully exploiting more advanced process technologies without themselves becoming experts in the physics of those technologies.

Even with relatively recent process technology generations, design teams could expect reasonable silicon yield if they complied with the few hundred rules in typical design rule decks. In turn, companies could count on quickly ramping up production to achieve production yield in new designs comparable to the nominal yield of the production line.

At 130nm and below, however, silicon foundries were forced to add significantly more rules to account for a growing impact of manufacturing on silicon performance. The flood of detailed rules continued as the industry moved to even more advanced nodes. As a result, some processes today require design decks with over 10,000 lines of rules. Yet, even with the explosive growth in design rule complexity, semiconductor companies continue to struggle to find accurate measures of silicon yield for any particular new chip. Even the largest rule deck simply cannot anticipate all the physical effects of manufacturing at very fine dimensions *(See Figure 1)*.

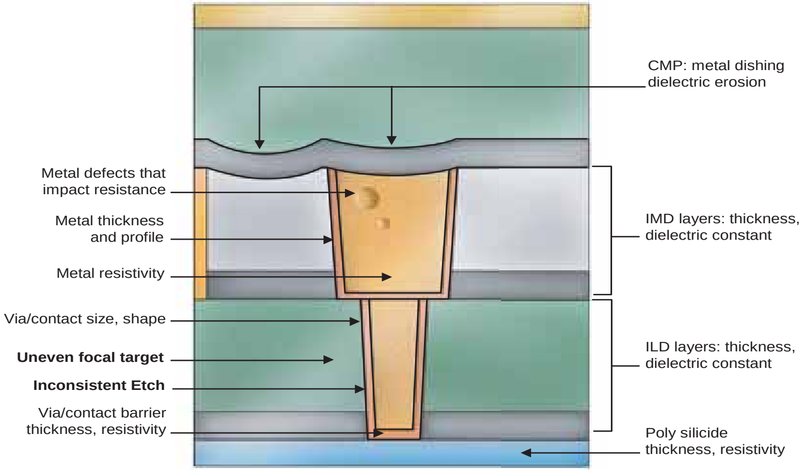

Figure 1. At finer geometries, a growing array of manufacturing effects begin to contribute to process-induced variations that can dramatically affect silicon performance.

TRADITIONAL METHODS

Created to simplify the relationship between the designer and the fab, design rules are intended to reflect limitations of the physics of the manufacturing processes. In practice, design rules represent a snapshot in the tradeoff between design schedule and manufacturability *(See Figure 2)*. By adhering to stricter design constraints, a design team can improve the likely yield–but at a greater cost in time and resources needed to manage the rules and greater complexity. In fact, overly strict rules levy other costs such as increased area or power.

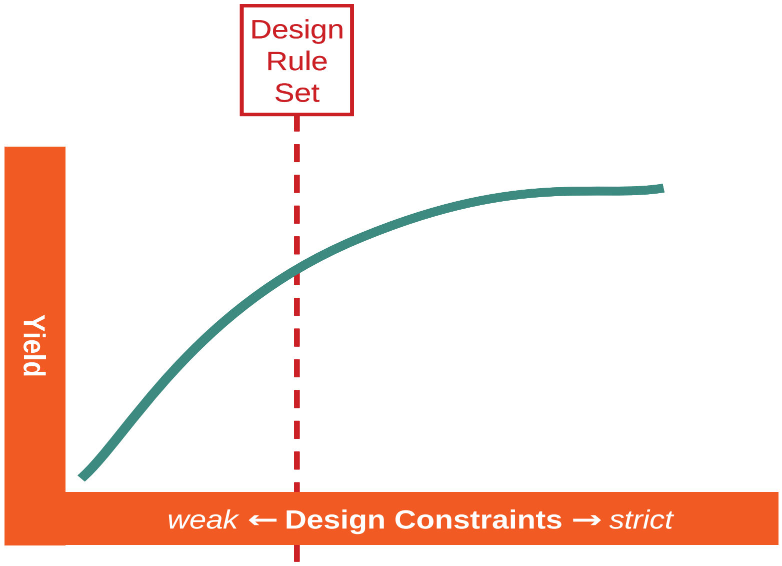

Figure 2. Design rules represent a specific tradeoff between speed and effectiveness. Stricter design constraints will improve the likely yield, but will force design teams to take longer to complete the design due to the larger number of rules and increased complexity.

Traditionally, the semiconductor industry has approached this tradeoff by creating rule decks withas simple and few rules as possible to speed execution, but then augment these minimal rule sets by adding some safety margin into the design constraints. This safety margin is intended to compensate for any imperfection in the rules and also cover any variations in the manufacturing process, but it brings its own costs. Increased margins can lengthen the design cycle as designers try to meet artificially tight timing budgets; furthermore, it inherently limits the design team's ability to take full advantage of the capabilities of the manufacturing process.

The use of a safety margin to compensate for manufacturing variations and simplified design rules remained an effective strategy while manufacturing effects were relatively small. Prior to reaching the 90nm node, the main manufacturing effects were via failures and particle defects. These effects are random in nature have been well managed by the semiconductor manufacturers. Below 90nm, other manufacturing effects from processes such as lithography and chemical-mechanical planarization (CMP) become too important to ignore–even dominating yield and performance at 45nm and below. These new effects are very much design dependent and as such are systematic, not random. This means that designers have the ability to increasingly impact the yield they can expect from their design.

As geometries shrink, lithography effects convert simple rectilinear layout shapes into complex curves with missing features and wrong dimensions. Intended to restore the desired shape, manufacturers manipulate the layout through the use of Reticle Enhancement Treatments (RETs). While these treatments are very effective they are imperfect and sometimes introduce their own artifacts or unintended shapes.

The Chemical Mechanical Polishing (CMP) process produces variations in metal layer thickness and contour across the entire wafer and across individual chips *(See Figure 3)*. These variations cause radical changes to the dimensions of wires, depending on the pattern, density, width, and other aspects of the layout. These dimensional changes can significantly impact performance or even the function of the design because they change the resistance, capacitance, and inductance of the wires. The amount of variation is surprisingly large–up to 30% variation in thickness and width. Worse, these variations are different for each different design. The specific layout shapes determine how each design and each layer is affected by CMP.

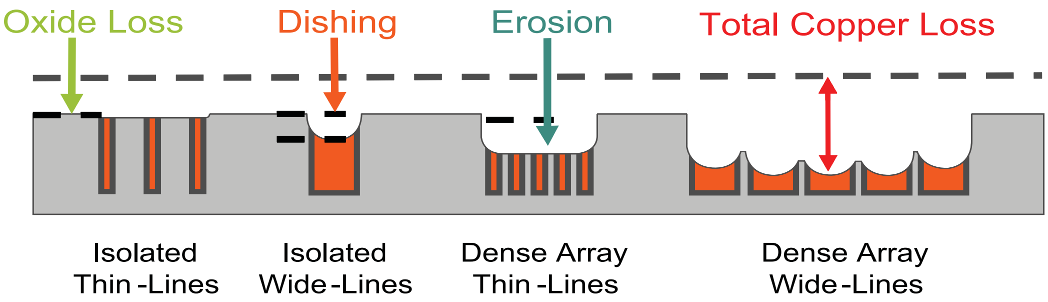

Figure 3. Chemical Mechanical Polishing (CMP) processes produce variations in layer thickness and contour across the entire wafer and across individual chips. These variations cause radical changes to the dimensions of wires, depending on the pattern, density, width, and other aspects of the layout.

Another impact of smaller geometries is that shapes that used to be independent now create interference for each other. For example, at larger geometries, the manufacturing effects produced by shapes inside one cell had limited impact on adjacent cells so the "halo effect" was limited to the cell boundary. When the same halo effect appears in a process with smaller geometry, however, its impact extends beyond the cell boundary and creates additional interactions that may not be caught by traditional design rules.

Individually, these effects and others introduce significant variations in the timing, power, and other parameters of the final chip. For many designs, these variations are too large to ignore and too large to hide within the safety margin of the design. At more advanced nodes such as 45nm, the interaction of these effects actually introduces new classes of problems.

INTERACTION EFFECTS

For example, lithography and CMP effects can interact to create far more yield problems than expected with the individual effects alone. At fine geometries, features are smaller than the wavelength of light used by the litho stepper, so the mask includes RET features such as sub-resolution assist features (SRAFs). The fab's responsibility is to make certain that the final silicon shapes are within size tolerances, using predetermined "cut lines" to measure these critical dimensions. A design team can run the layout through a litho process simulation to determine the range of exposure (called "dose") and the range of focus accuracy (called "depth-of-focus," or "DoF") that can be tolerated while still keeping the critical dimensions within the requirements. Each cut line produces an upper and lower curve on the chart marked "Common Process Window" on the left side of *Figure 4*. The open space in the middle is the range of dose and focus over which the litho process can vary, while still meeting all of the critical dimensions marked on the layout. While some litho variations occur due to equipment aging and to slight changes in the litho environment, other variations arise from differences between wafers.

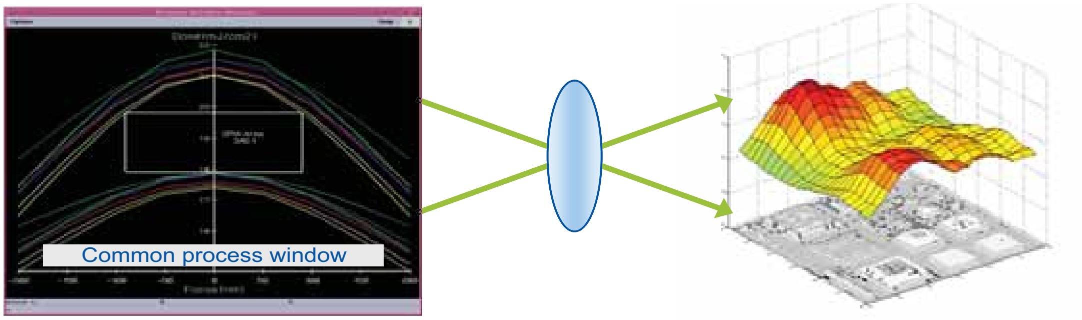

Figure 4. When variation in surface height due to CMP (right side of figure) is combined with the relatively shallow depth-of-focus of the litho process (left side of figure), some features of the layout will likely be distorted or even missing, resulting in parametric or functional yield failures.

From the litho point of view, the Common Process Window might seem sufficiently large to ensure that this particular layout with these RET features should print well despite some manufacturing variations in the litho process. In this example, the depth of focus range is +/- 100 nanometers for this small area of the layer–and would certainly be lower for a larger area. In fact, according to the 2003 International Technology Roadmap for Semiconductors (ITRS), the 65nm node requires site flatness of 64nm or better.

Complex interaction problems arise when the mask is projected onto a real chip surface, which in practice is almost never truly flat. The surface height varies from chip to chip across the wafer, and it varies within each individual chip depending on all of the CMP-induced effects associated with previous layers. As noted earlier, CMP flattens the surface between processing steps but is itself affected by the mix of shapes on each layer. The result can easily be 100nm variation in surface height within a chip layer. Combined with this variation in surface height, the relatively shallow depth-of-focus of the litho process will most likely result in distorted or even missing features–and parametric or functional yield failures.

ALTERNATIVE APPROACHES

In one current approach to account for increasing manufacturing effects, fabs have introduced a second layer of rules, called recommended rules. These rules are usually stricter and more complex, increasing design tool runtime–and therefore lengthening the design cycle. For example, a "required" copper density rule might specify maximum and minimum copper density within tiles of a certain size, such as 20x20 microns, with an overlapping pattern to ensure full coverage. A "recommended" rule might include stricter max and min, smaller tiles, and a more dense overlap pattern. In practice, because the value of the rule is less certain, the recommended rules are often considered simply optional.

Adding more rules, however, does not address the fundamental limitations of a rule-based approach. Designers still must deal with too many rules, too-strict rules, and too much margin. Furthermore, rules do not easily handle interactions of effects, such as the litho-to-CMP connection described earlier–and designers face other interactions such the increased halo effects at subwavelength geometries. For example, when OPC or RET techniques are applied to two adjacent blocks–even blocks that meet all design rules–the litho treatments can create surprise artifacts that can affect the performance of the circuit.

In another example of unanticipated interaction, the application of routine CMP processing to several layers that are individually DRC-clean can stack up–allowing a soft spot that is severely eroded, changing parasitic resistance and capacitance, and even allowing metal pooling that causes a short circuit *(See Figure 5)*. More fundamentally, rules are always a compromise between two types of errors–false negatives (Type I) and false positives (Type II).

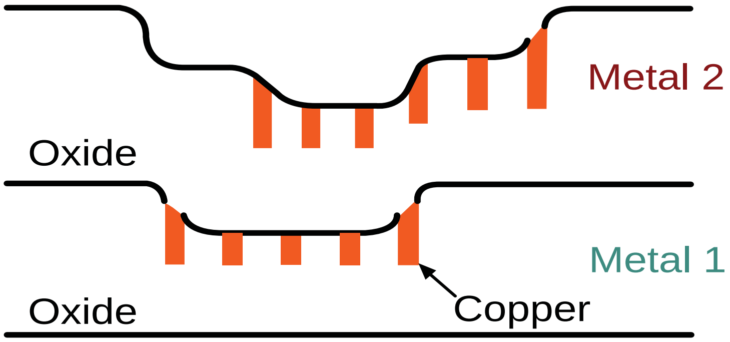

Figure 5. Even recommend rules cannot easily handle interactions of effects such as the unanticipated interaction when routine CMP processing applied to several layers that are DRC-clean stacks up, allowing a soft spot that is severely eroded, changing parasitic resistance and capacitance, and even allowing metal pooling that causes a short circuit.

For example, a Type I error might arise when design rules do not anticipate an interaction between the layout shapes and the RET scatter bars that causes an artifact to appear. The shape might be harmless, or it might cause changes in parasitics that cause failure in the circuit.

A Type II error might arise when rules catch a via that is vulnerable because it is embedded in a narrow wire. The rules require an increase in the via "surround" so theoretically it is more tolerant of manufacturing variations. But those changes block the use of scatter bars around the via, which actually makes the area more vulnerable to manufacturing variations. Although the original error might not have been false, the layout change that it precipitates is certainly a dubious, or even false, optimization.

MANUFACTURING MODELS IN DESIGN

A better solution for handling systematic manufacturing variations is to add modeling technology in the design flow (Figure 6). Models do not replace rules, but they do enable tradeoffs and optimizations in the design process that cannot be achieved with rules alone. Rules offer only one or two points of reference that can sometimes be misleading. In contrast, an executable model can better illuminate the risks and costs of an important design decision. In fact, for highly-optimized designs, a design team might even employ models for several manufacturing processes to achieve the best overall result. Employed in conjunction with rules, models provide improved results quickly, while maintaining consistency with more detailed versions of the same models needed for signoff.

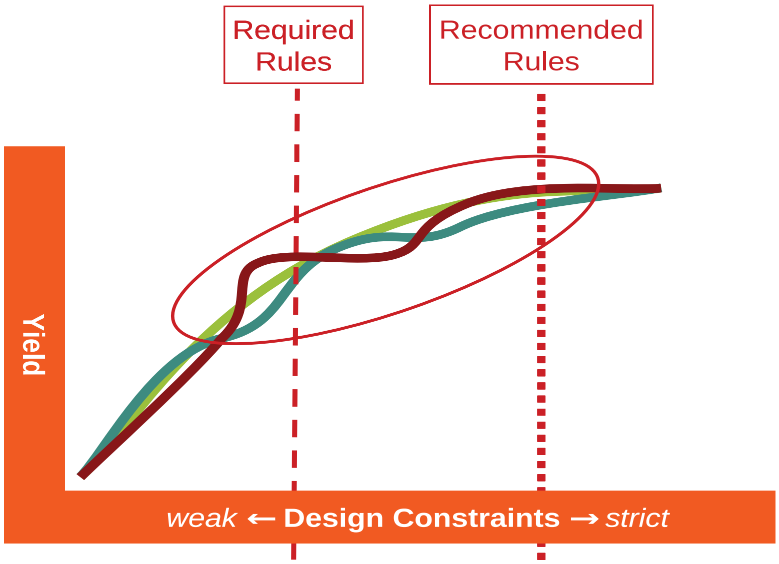

Figure 6. The use of modeling technology in design flows provides a better solution for handling systematic manufacturing. Models do not replace rules, but they do enable tradeoffs and optimizations in the design process that cannot be achieved with rules alone.

Previous applications of manufacturing models in design flows met with limited success at best because the only available models, TCAD models, were highly-detailed–and therefore slow. The degree of detail in these models not only made them slow, but also posed a risk to the fab because the details contained confidential information about the fab process.

Newer abstraction techniques deliver models that provide both confidentiality and enough speed to use within the design cycle. Emerging manufacturing models will operate in design flows transparently without requiring a great deal of knowledge of downstream manufacturing processes. Today, customers who are designing at 65nm and preparing to design at 45nm have started employing CMP and lithography models into their design flows. By using these models, they are able to understand the manufacturing effects on yield and performance in the context of their design.

This enables designers to remove excessive guardbanding required in a strictly rule-based approach. For example, extraction models may add up to 15% delay margin to account for the variability of thickness due to CMP. By applying a CMP model, designers can remove the 15% guardband and apply the actual impact of CMP to their timing. This methodology can significant shorten the amount of time required for timing closure and allow customers to tape-out much sooner and reducing the risk of costly design respin.

DESIGN FLOWS

Within physical-design flows, model-based methods will complement rules-based methods, providing design teams with another important tool for iterative design refinement. In fact, engineers will likely exploit the speed of rules-based systems for early design work. Later, during more rigorous analysis, more accurate model-based methods would be focused on specific parts of a design that require closer attention. During subsequent iterations, the design elements modified through such deeper analysis would be "fixed", preventing introduction of Type II errors by faster but less accurate rules-based systems. This differential application of model-based deep analysis tools to select portions of a design highlights a key principle of emerging design flows–that of not only applying the right tool for the right job, but also applying the right tool to the right part of the job.

A powerful application of this technique is to test and qualify library cells for litho correctness before they are signed off into the design library for general use *(See Figure 7)*. Any type of litho treatment can be qualified with this procedure. Rather than storing the treatment with the cell, this approach ensures that the cell will be treatable in the final chip design when it has been instantiated hundreds or thousands of times.

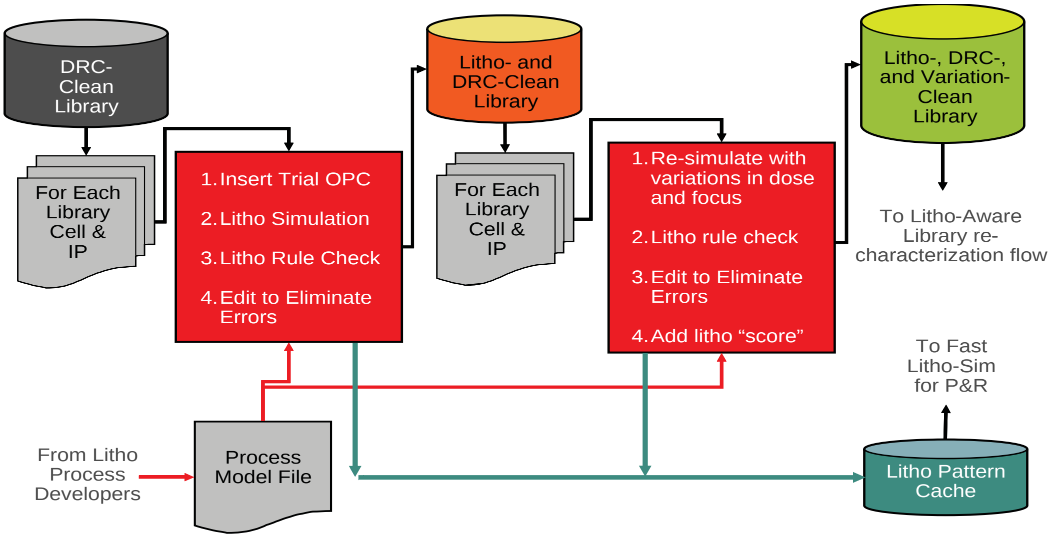

Figure 7. A model-based approach would allow designers to test and qualify library cells for litho correctness before they are signed off into the design library for general use.

Within the Cadence Virtuoso® layout environment, the overall procedure is similar to design rule checking, where the designer can immediately change whatever is necessary in the layout window. Here, the router interactively sends a set of shapes to the model-based analysis tool, providing quick feedback on potential manufacturing problems.

Another application of model-based methods in physical design uses CMP modeling of design-specific thickness variation for improved parasitic extraction *(See Figure 8)*. Here, critical layers of the layout are first modeled by the CMP engine to create a thickness profile of each layer. The Cadence CMP engine is the leading commercial solution for CMP modeling and has been validated by a number of leading fabs and foundries. Along with the design, this layer thickness data is fed into the QRC extractor, which uses the thickness information to extract parasitics based on actual wire dimensions in each local area, rather than general approximations. The accurate parasitic information is made available to all of the design tools that rely on parasitic information: simulation, timing, IR drop, signal integrity, and others. The improved accuracy of the parasitic values thus leads to improved accuracy in many critical steps that determine the success of the design and the yield of the chip.

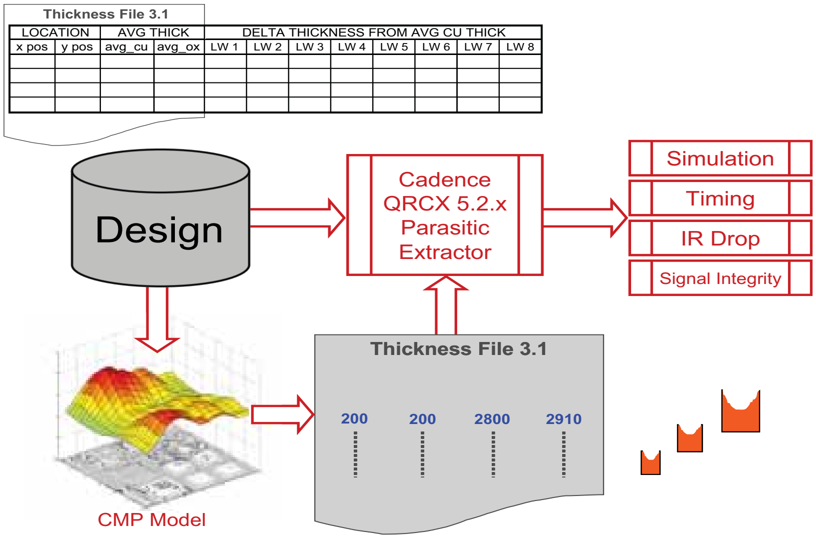

Figure 8. Incorporated into Cadence design flows today, CMP modeling improves accuracy of the parasitic values, which leads to improved accuracy in many critical steps that determine the success of the design and the yield of the chip.

CONCLUSION

Despite an explosive growth in design rule deck size and complexity, design teams are forced to deal with the fundamental limitations of rule-based approaches. With the emergence of model-based methods to complement existing rule-based systems, engineers can inject manufacturing knowledge early in the design process in a transparent and flexible fashion. Like design rules, manufacturing models will continue to emerge at the different levels of abstraction needed for different phases of design and verification. Using this approach, semiconductor companies can improve time to volume manufacturing, time and predictability with design methods that are truly correct-by-construction.

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info@cadence.com

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Cadence Design Systems, Inc.

CORPORATE HEADQUARTERS
2655 Seely Avenue
San Jose, CA 95134
P: +1.800.746.6223 *(within US)*
+1.408.943.1234 *(outside US)*
F: +1.408.943.5001
www.cadence.com

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