

FRONT-END LOGIC DESIGN:
TAKING THE RISK OUT
AND PUTTING SCHEDULE
PREDICTABILITY IN

INTRODUCTION

All successful digital chip projects rely on the front-end logic design team—not only to create the logic from architectural specifications but also to ensure that it is functionally correct and ready for effective back-end implementation. Without sound logic design, the program can be fraught with problems, delays, and failures. In other words, how a project starts is instrumental in its ultimate success or failure.

Interestingly, today’s logic design flow process and tool technologies are still largely a byproduct of haphazard evolutionary flows offered by the previous generation of front-end technologies used in the marketplace, which have not kept pace with the emerging challenges.

Over the last few years, the ever-growing design complexity and design challenges associated with criticality of power, growing design-verification gap, inefficiencies of the logical-physical iterations, lack of clear implementation test and validation checkpoints, and the unpredictable nature of the ad-hoc iterative design process, have created the need for a fundamental shift in the way design is done.

The result of the mounting challenges in design, coupled with the piecemeal evolution of design methods has led to a crisis in the schedule predictability of chip programs. For example, *Figure 1* shows data gathered by a systems design company in Japan. The company has analyzed project data from five generations of projects in which overall complexity has grown 13 times. The number of tool inter-dependencies and resulting iterations when using an ad-hoc serial approach were creating a situation where the schedule variability was actually greater than the original project schedule itself.

ADDRESSING DESIGN TEAM CHALLENGES

As shown in *Figure 1*, the challenges facing design teams ultimately manifest themselves as major upheavals in the development and business planning process. In order to combat these effects, logic design teams must start addressing the key risk areas that are contributing to the predictability crisis, and do so early and in a metrics-driven concurrent fashion.

Figure 1: Schedule Predictability Crisis

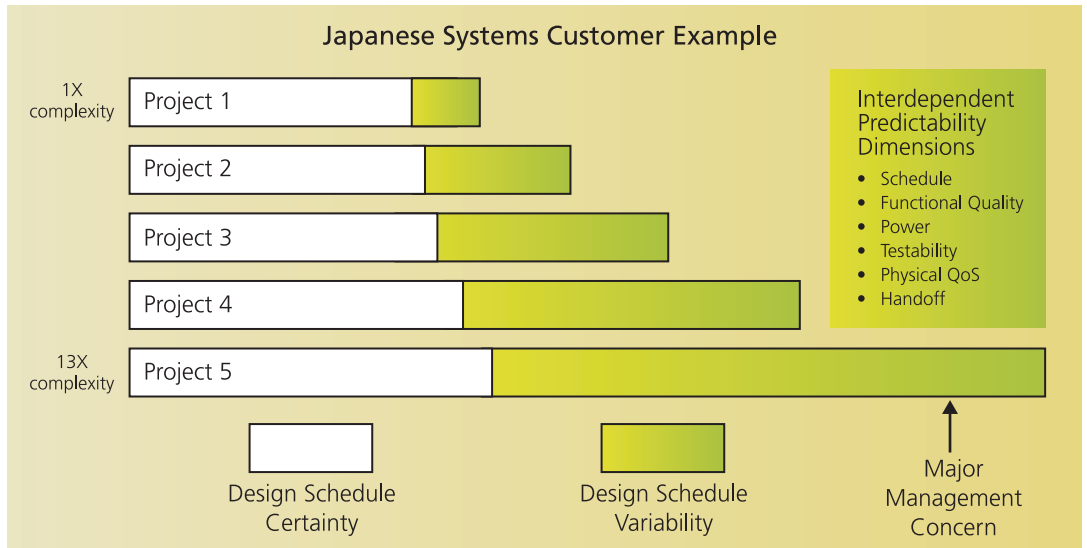


Figure 2: Key drivers of changes to the front-end design flow and relationship between the drivers.

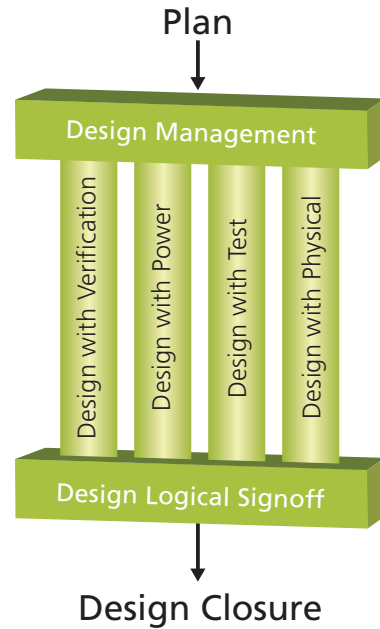
Interrelationship of Drivers of Change				
	Power	Verification	Test	Physical
Power	Leakage & dynamic power trade-offs must be made in context of broader timing, die size and schedule requirements.	Verify power modes in functional operation; correctness of power structures.	Power-aware design-for-test and automatic test pattern generation (power during test; test of power structures).	Accurate power estimation requires accurate capacitance data. Power grid modeling effects increasing.
Verification		Integration levels enabled by Moore's Law make every generation more challenging.	Growing relationship between testbench and test program generation and reuse.	Timing modeling importance in architectural feasibility analysis increasing => better physical modeling needed.
Test			New challenges posed by increased interconnect failures means changes to DFT and ATPG methods.	DFT structures having more impact on physical design (e.g. congestion): physical data needed to drive accurate delay test.
Physical				Modeling of physical effects critical to push forward because many decisions hinge on accurate modeling/analysis.

The key culprits are summarized in *Figure 2*. Power has emerged as a leading design concern that permeates all aspects of design planning and project execution. The exponential nature of the verification problem is no secret, but the growing interrelationship with other aspects of design is yet another dimension to its complexity, and tail-end verification alone is just no longer enough. Test, often an afterthought, has new requirements that are forcing broader visibility, earlier in design processes. The physical attributes of the latest process nodes bring greater importance to getting some measure of physical modeling as early as possible into the design flow.

Minimizing risks faced by logic design teams means upgrading the front-end flow from the haphazard evolutionary set of technologies of the industry's current front-end offerings. A new approach to solving growing challenges is needed, addressing flow bottlenecks and inefficiencies in standard production flow with a metrics-driven flow, where engineering teams concurrently design "with" verification, power and other factors in mind. The right solution for logic design teams can address these challenges and reduce overall risks with:

- **Design with Verification** — delivers on the promise of early verification by design teams to shorten the overall time to market, while significantly raising design functional quality and reducing risks of late and costly design iterations with ripple effects.
- **Design with Power** — brings the first power-aware design, verification, and implementation flows to market, moving power from an implementation care-about into an early design and verification consideration.
- **Design with Physical** — reduces the logic-physical late iterations by bringing production silicon virtual prototyping into the synthesis environment.
- **Design with Test** — accelerates development of high-quality test infrastructures and enables design teams to minimize cost of test.
- **Design Logical Signoff** — aids with back-end handoff checkpoints for design teams to achieve front-end signoff closure quickly and accurately, thereby improving quality.
- **Design Management** — provides a plan and metrics-driven flow across the entire design and verification tool set, bringing unparalleled predictability from plan to closure, while reducing flow redundancies and minimizing iterations.

Figure 3: Logic Design Team Solution Architecture



- **Design with Verification**
 - Early verification by designers to shorten overall time to market
- **Design with Power**
 - Power-aware design and verification flow
- **Design with Test**
 - Test-aware early front-end design
- **Design with Physical**
 - Reducing logic-physical iterations
- **Design Logical Signoff**
 - Ensuring proper design handoff to the back-end
- **Design Management**
 - Risk reduction with predictability for ad-hoc process

With power, verification, test, and physical modeling design issues becoming increasingly intertwined, it is rare that a design team can re-cast existing design flows to truly attack one of these issues on its own. A holistic approach is critical to achieving a successful outcome.

TAKING THE RISKS OUT OF FRONT-END LOGIC DESIGN

While all these issues are virtually inseparable, some further background on each should help to catalyze a clear path to action.

DESIGN WITH POWER

Design with Power is needed, as power has become a ubiquitous design issue, nearly independent of the end IC target market. At 90nm and below, a majority of logic design teams are using at least one new design technique to mitigate power dissipation. There are a litany of known techniques for reducing power consumption; however their implementation has been labor intensive, risky, and, for the most part, relegated to the back-end of the design process. The ideal solution for low-power design enables design, verification, and implementation of advanced low-power design techniques using a full solution approach that thereby reduces the effort and risk associated with the application of multi-supply voltage and power shut-off design techniques.

DESIGN WITH VERIFICATION

Design with Verification is needed as it is no secret that functional errors are the main source of silicon re-spins. As Moore's Law marches forward, functional verification complexity follows its own exponential growth path. The idea that verification needs to start as early in the design flow as possible—ideally as the RTL is just being created—to help logic design teams bring up RTL blocks faster and with greater quality is gaining broad market acceptance. This further complements and eases the efforts of dedicated verification teams. Moreover, effective early functional verification starting with formal analysis—followed by simulation and then hardware-based acceleration techniques, with metric driven verification management—directly impacts design team productivity and quality, reducing the time to market, and proving the old saying that “an early bug is a cheaper bug.”

DESIGN WITH PHYSICAL

Design with Physical is needed as physical modeling issues have been challenging design teams since the transition from .25-micron to .18-micron technologies. The problems have been exacerbated with the introduction of each new process node. The handicaps of the incumbent solutions have led design teams down two principal roads: either ignore interconnect all together (i.e., use zero wire load models), or take responsibility for some of the aspects of physical design themselves (i.e., hand-off post physical synthesis placed gates). Both of these approaches merely skirted the issue of better interconnect modeling in the front-end design process. The new solution directly improves the interconnect modeling, leading to fewer iterations and better designs.

DESIGN WITH TEST

Design with Test remains an important aspect of correct design implementation, with the design for test consideration being crucial up-front in the design process instead of proceeding with an error-prone post-netlist process. The ability to accelerate the development of a high-quality test infrastructure enables design teams to minimize cost of test.

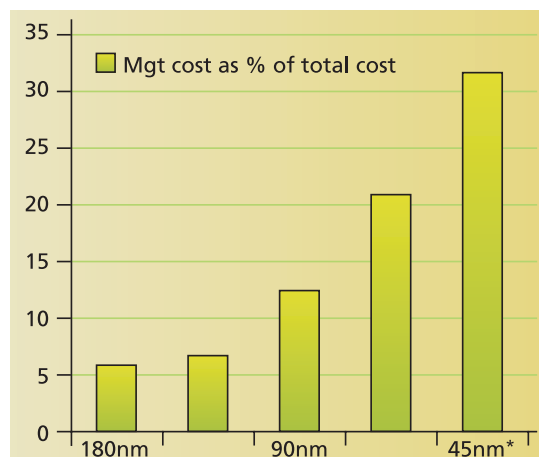
DESIGN LOGIC SIGNOFF

Design Logic Signoff is another must-have for effective design process, enabling design teams to provide a clean front-end handoff to the back-end process. Leveraging linting and structural diagnostics, equivalence checking, timing constraint validation and static timing analysis checkpoints helps design teams achieve front-end signoff closure quickly and accurately, improving overall quality.

DESIGN MANAGEMENT

Design Management is all about bringing metrics into a process, thus allowing for meaningful project tracking and refinements. The same concepts apply equally well to logic design, where today costs associated with program management alone are projected to continue to skyrocket as organizations try to address the growing problem, unless new methods that provide visibility and predictability to the design process are not adopted. Design Management is a must as the plethora of technologies used by logic design teams, along with tool interdependencies in a serial flow, results in an ad-hoc and unpredictable process where it is hard to plan and track execution progress. By extending the verification management capabilities into design, up-front executable planning with both design and verification metrics and milestone based tracking provides a high degree of predictability, highlighting critical paths. Also helping project managers reduce the risks associated with complex ASIC and SOC design, and enabling a complete flow management process from plan to closure.

Figure 4: Design management





CONCLUSION

In this paper we presented a set of targeted solutions for logic design teams aiming at reducing the overall risks associated with front-end logic design and verification while reducing the inherent risks. Mounting data (see *Figure 1*) supports the critical need to take action if the resulting schedule predictability crisis is to be averted. Those teams that do make the tough decisions for change will be rewarded with capabilities to make more competitive designs faster and cheaper, with a critical advantage in design process predictability and shipping products to market on time or ahead of time.

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