



USING PARASITIC-AWARE  
SIMULATION IN THE DESIGN  
AND VERIFICATION OF COMPLEX  
RF SIP MODULES

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## INTRODUCTION

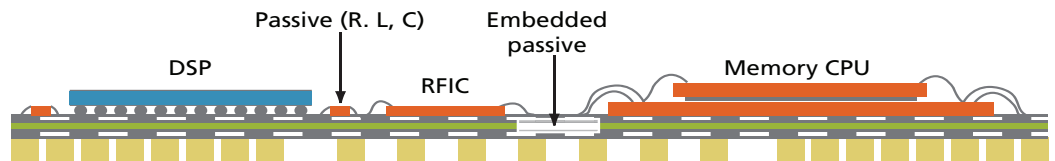
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The key advantages of SIP designs—a high degree of flexibility in package architecture and the ability to mix and match IC technologies—also create some of the biggest challenges during verification. Add to this the complexities specific to RF designs, and designers need a verification capability that supports elements unique to RF SIP designs.

## SIMULATION CHALLENGES OF RF SIP DESIGN ELEMENTS

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In an RF SIP design, a single package substrate is used to integrate digital ICs, logic ICs, and RF ICs plus SAW filters, mechanical parts, and passive components. The package substrate serves as a system integration vehicle and might contain passive elements. (See *Figure 1*)



*Figure 1. RF SIP Design*

Broadly, three key technology- and topology-based RF SIP features make the RF IC simulation environment inadequate for RF SIP simulation, making it necessary to include special analysis and verification techniques. These features are:

- Multiple process technologies
- Passive integration
- Package interconnects

## MULTIPLE PROCESS TECHNOLOGIES

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An RF SIP design is made up of components of various technologies. Even the package substrate, which integrates the components, is based on a different technology. Therefore, RF SIP simulation must support concurrent simulation of disparate technologies.

## PASSIVE INTEGRATION

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RF SIP designs extensively use passive integration to miniaturize systems and reduce costs. Passive components also play a key role in RF designs in performance matching, tuning, filtering, and biasing. Two passive integration techniques that are commonly used in RF SIP designs are integrated passive devices and embedded passives.

Integrated passive devices are typically thin-film solutions of resistor and capacitor arrays connected to the package substrate like other SIP design components through wirebond or flip-chip technologies. Embedded passives, on the other hand, are passive components integrated in the package substrate and therefore need to be analyzed carefully for high-order effects, such as dispersion and radiation.

To speed up the design process, it is critical that in the explore stage of designing itself the designer has the capability to synthesize passives and generate models with various levels of accuracy.

## PACKAGE INTERCONNECTS

SIP layout traces and wirebond or flipchip connections to package pins constitute the package interconnects in an RF SIP design. These interconnects significantly compound design complexity and increase simulation challenges when compared to RF IC. In RF SIP simulation, trace metal thickness and 3D modeling of package interconnects become more important than in RF IC simulation. While RF IC designers extract just the R and C values of a line, usually with quasi-static solvers, RF SIP designers need to capture transmission-line effects with full-wave EM solvers for interconnects as well as embedded passives.

## TRADITIONAL RF SIP SIMULATION

Traditional RF SIP simulation relies on RF IC simulation environment and simulator capabilities. As RF IC simulation does not take into account both SIP- and chip-level perspectives, it cannot be used to verify or optimize RF SIP designs accurately or completely.

Another key problem that RF SIP designers face when using traditional simulation methods is that these methods do not provide an easy way to conduct a partial simulation of a design. Many a time, RF SIP designers are interested in simulating and analyzing only a portion of the design. The need for a partial simulation can be many. Because an RF SIP design contains multitechnology dies, embedded passives, interconnects in a single package, the design might become too big and complex for a system simulation. Or the analysis of a critical design might require a portion of a silicon die to be simulated with a portion of an RF SIP module. In other cases, the designer might want to decide on component values or routing topologies together with parasitic information extracted out of a partial or complete SIP layout. (See Figure 2)

Regardless of the need, the traditional approach to partial RF SIP simulation is manual and error-prone. In addition, it requires the designer to maintain several copies of different partial circuits created from the original design and sync-ups across several copies often become unmanageable.

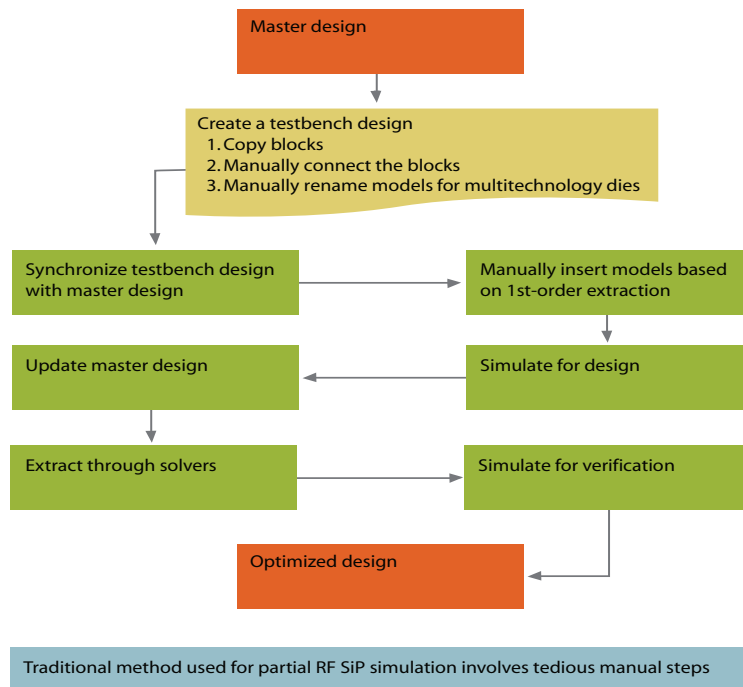


Figure 2. Traditional RF SIP Simulation Method

To begin a partial RF SIP simulation, the designer first needs to create the testbench design. In the traditional method, testbench creation is a three-step process that involves several manual and time-consuming tasks. The designer first copies the required blocks or components from the master design. Next, these blocks or components are manually connected as in the master design. The designer then needs to manually rename models across the different technology nodes. This is a tedious task and a significant productivity buster.

After the testbench is created, the designer must run trial simulations to ensure that all required components have been copied from the original circuit for simulation to occur properly. The testbench design is synchronized with the master design during this step.

Next, based on first-order extraction, models that represent layout parasitics have to be manually inserted in the netlist or the schematic. This step is also tedious and time-consuming because it requires manual abutment of nets and insertion of parasitic models.

At this stage, the designer can simulate the testbench design and tune the master design based on simulation results.

Next, using third-party solvers, the designer needs to extract physical nets and embedded passives from the master design. In most cases, the third-party solvers are not well-integrated into the SIP flow and therefore the methodology for extraction is cumbersome and time-consuming. Finally, the design is simulated for verification.

## PARASITIC-AWARE SIMULATION

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An automated verification flow that supports the process of extracting critical portions of the design and allows simulation of this partial design together with parasitic effects from the layout is the need of the hour. The simulation environment and the simulator should have the capability to support a variety of models (transistor-level, HDL, S-parameters, and transmission lines), bends, tees, tapers, and so on because a SIP design is a conglomerate of all these.

The simulation environment needs to enable quick and fast first-order approximations as well as extractions through full-wave solvers for spiral inductors, 3-D wirebonds, and 2-D layout shapes, such as tapers and bends.

Because dies on a SIP can be on different technology nodes and characterized for different nominal temperatures, it is important that the simulator is able to simulate multiple such dies without the need for renaming models and with the option to specify a temperature local to the die subcircuit.

## CADENCE RF SIP SOLUTION

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The RF SIP solution from Cadence offers an integrated environment for design, implementation, and parasitic-aware simulation of RF SIP designs. The solution makes it easy for the designer to do partial simulations by automating various tasks. Let's examine the task flow in the case of partial simulation done with the Cadence RF SIP solution. This flow has four key phases:

- SIP testbench creation
- Net and passive extraction
- Parasitic backannotation of layout-extracted models onto testbenches
- Analog simulation

## SIP TESTBENCH CREATION

As in the traditional flow, the designer first creates the testbench design from the original design. However, instead of copying the required blocks, the designer can simply extract the blocks. Using the Cadence RF SIP solution, the designer can mark critical blocks at all levels of a hierarchical design on the graphical canvas or in table view. (See Figure 3)

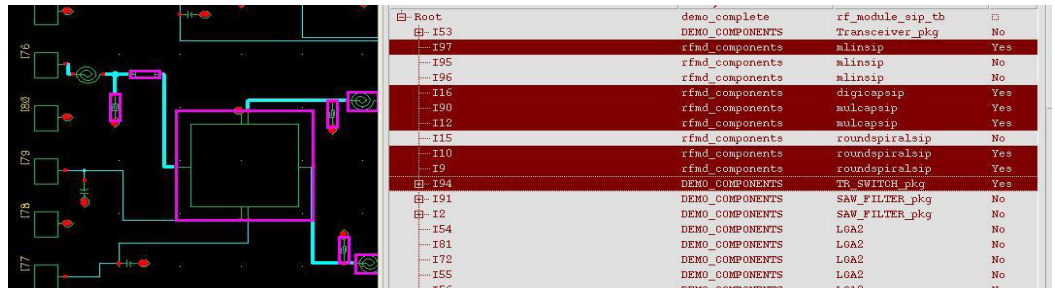


Figure 3. Marking critical blocks on the graphical canvas and in table view

The embedded passives that need to remain connected to the subdesign selected for extraction get selected automatically.

When the testbench design is extracted, the selected blocks or instances get extracted into a new design with their connectivity maintained. Because the circuit is a portion of a complete design, it has nets that remain floating or unconnected. These nets and the global nets become interface ports for the designer to hook in relevant biases and input stimuli.

## NET AND PASSIVE EXTRACTION

In the Cadence RF SIP solution, the solvers are integrated into the flow both at front-end design entry and SIP Layout levels. While front-end integration enables solvers to run in quick mode and provide first-order models for early design exploration, the backend links provide a way to extract detailed parasitic models for nets and passives.

This integration of the Solver technology into a single environment for IC and SIP design enables the designer to analyze passives in SIP or silicon and bring in both SIP- and chip-level perspectives into RF SIP design.

## PARASITIC BACKANNOTATION OF LAYOUT-EXTRACTED MODELS ONTO TESTBENCHES

In this phase, the designer does:

- Annotation of First-Order-Estimated Models
- Annotation of Models from Solver-Based Extraction

### Annotation of First-Order-Estimated Models

Annotation of first-order-estimated models involves analyzing SIP passives to generate closed-form-equation-based models and doing a first-order annotation of SIP routes. This process abuts the layout route into a series of known RF shapes, which can be inserted into the schematic design as a subschematic of RF elements connected together. While the results are not accurate, the method is quick and easy and works well for estimation.

### Annotation of Models from Solver-Based Extraction

If the designer runs solvers on critical nets, the designer can import higher-order models to the schematic. The associated nets get abutted and the parasitic model gets inserted automatically. Then, a symbol gets created for the testbench design that has pins corresponding to interface ports. Using this symbol, the designer can hook the testbench with stimuli.



The Cadence RF SIP flow eliminates the need for:

- Capturing designs twice for purposes of simulation and SIP implementation
- Creating separate testbench designs for analysis and simulations, followed by manual sync-ups with the master design
- Manual insertion of parasitic models (obtained from third-party sources) into the testbench design
- Manual renaming of models for different dies that are on different technology nodes
- Explicit export of layout structures to third-party solvers for extraction

## ABOUT THE AUTHORS

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