



RF DESIGN METHODOLOGY  
AND FLOW



WHITE PAPER

## OVERVIEW

This document describes the wireless RFIC reference flow as part of the Cadence® RF Design Methodology Kit. Cadence Kits address application-specific design issues by combining a verified methodology packaged in platform flows, with enabling and standards-based IP—all applied to a market representative reference design. The AMS and RF Kits target full custom designs across the diverse design domains of analog, custom digital, and RF. The Kits also integrate IP from these diverse domains, including importing digital standard cell blocks with an integration strategy and methodology.

The underlying AMS and RF flows are based on an overarching methodology that deals with each design domain and subsequent integrations, and that is designed to serve as a “blueprint” against which any platform targeting custom design can be measured. The RF Design Methodology Kit is based on the Advanced Custom Design Methodology (ACD) and constitutes one of the kits associated with the end-to-end wireless design problem.

## THE ADVANCED CUSTOM DESIGN METHODOLOGY

Represented in Figure 1, predictability is the driving force behind the ACD Methodology. Predictability is predicated on two primary concerns: that schedule is met from the beginning of the design process (necessitating a fast path to tapeout), and that performance requirements are met to achieve first-pass success (requiring silicon accuracy).

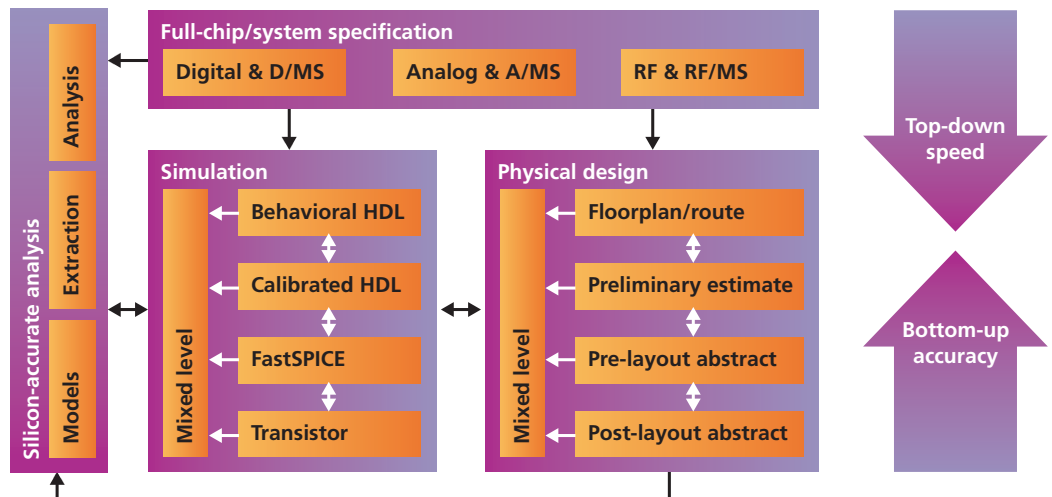


Figure 1: The Advanced Custom Design Methodology

Meeting schedule requires a fast design process that supports thorough and complete simulation and physical design. The design process is comprised of many tasks, and many of today’s chips contain multiple blocks from multiple design domains. Thus, it is imperative to design in as many of these blocks and perform as many tasks as possible in parallel, leveraging as much of the top-level IP throughout the process as possible. This leads to the concept of design evolution, wherein all design IP is leveraged as it matures through the design process. The top-down design process, when applied to both simulation and physical design, is the approach that facilitates a fast design process.

Multiple abstraction levels, from high-level design through detailed transistor-level design, are combined to support a mixed-level approach that targets detailed design to only the points needed for a given test. This allows for leveraging the top level and using that information for block design, and subsequently re-verifying the blocks in the top-level context.

At the other end of the spectrum is the need for silicon accuracy to achieve the required design performance. Silicon accuracy relies on the base design data (such as device models) supporting accurate simulation, and on technology files supporting interconnect, physical verification, and analysis. Test chips, which often comprise critical structures known in the past to be highly sensitive, are also used in this process to verify the feasibility of a process and the accuracy of its corresponding process design kit (PDK). Often, a design group will need to add components to the PDK to support a particular design style. Device models may need to be expanded upon to either combine or add corners, statistical modeling, or other approaches the design team needs.

The silicon accuracy data is driven through the design process by detailed transistor-level analysis, including layout extraction. This comprises the lower level of the abstraction chain, which then supports the calibration of these results to higher levels of abstraction. This represents the bottom-up design portion of the ACD Methodology.

The top-down and bottom-up processes work in parallel to produce a “meet-in-the-middle” approach. It is this approach that balances the need for speed through the design process with the need for silicon accuracy, ultimately producing a predictable schedule that leads to first-pass success. The ACD Methodology can be applied to a complex integration or a particular domain area. Each domain applies the meet-in-the-middle approach, combining top-down speed with bottom-up silicon accuracy.

## THE RFIC CHALLENGE

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The demand on mobile communication has grown exponentially over the last few years. Today's mobile communication systems use sophisticated signal processing to achieve high transmission rates. The challenges for leading-edge wireless systems will increase even further, when designs must be targeted to multi-standard and reconfigurability. Evaluations of various integration strategies must be performed to verify the feasibility of the proposed integration approach, where issues such as performance, cost, and risk need to be considered.

The requirements of the varying communication standards differ over a wide range in terms of center frequency, signal bandwidth, signal-to-noise ratio, and linearity. This will have an impact on all radio front-end building blocks and will require comprehensive tradeoff analysis to select the most appropriate architecture and derive the individual circuit block requirements.

The complexity of digital signal processing is also steadily growing. Digital blocks offer the capability to compensate for some of the signal impairments caused by analog front-end blocks. To verify complicated digital compensation algorithms and the effect of analog non-idealities such as phase noise, non-linearity, and mismatch, the analog and digital blocks need to be simulated together. A key bottleneck in RF/baseband co-design is the presence of the RF carrier signal at several gigahertz in the RF front end. To simulate the bit-error-rate (BER) or package-error-rate (PER) of a complete telecom link at the transistor level—running thousands of cycles of the modulated signal—is very expensive and often impractical.

Aside from this performance verification, where the actual design is validated against specification, another key requirement is the functional verification of the entire chip. Simple implementation errors at the interface between the digital control circuitry (responsible for various operating modes like power up, power down, receive, transmit, and band selection) and the analog front end are often the cause of expensive re-spins.

IC designers typically overcompensate and stick to budget requirements passed down from the system designer. The IC designer may be able to prove that a more relaxed specification within the IC will still meet system-level requirements; yet, with no way to prove theory, time is spent optimizing circuitry that may not be necessary. Systems involving baseband and analog/RF portions have traditionally been designed, simulated, and verified separately due to the different mindsets

of the engineers and the tools of the two domains. The goal during system-level design is to find an algorithm and architecture that implement the required functionality while providing adequate performance at minimum cost.

RFIC designers also face several significant challenges during the actual implementation phase. Considering a large IC such as a wireless transceiver, high-speed requirements make circuits extremely sensitive to parasitics, including parasitic inductance, passive modeling, and noise. Thus, the essence of the RFIC flow is the ability to manage, replicate, and control post-layout simulations and effects, and effectively use this information at timely points throughout the design process.

RFIC design also requires specialized and unique analysis techniques specific to RF design. These are a cross between frequency domain and time domain analysis methods, which are chosen on the basis of either circuit type and type or designer preference and comfort level. Ultimately, this requires a seamless environment that allows a choice in simulation method.

Integration trends have also affected the RFIC world, which used to be viewed as a separate, almost standalone entity. Today, many RFICs contain at least the ADC, DAC, and PLL functions, as well as a digital synthesizer that is created through the digital environment and integrated on chip. In other cases, RF content is being added to large SoCs as some design groups attempt a single-chip solution. Still others are integrating by using system-in-package (SiP) techniques, which leads to similar verification issues as RFIC and SoC methodologies.

Addressing these challenges requires a complete solution that must:

- Provide comprehensive links between system-level design and IC implementation
- Enable IC verification within a system-level context to leverage the existing wireless libraries, models, and testbenches
- Allow full-chip mixed-level simulation at different abstraction levels (language neutral)
- Allow for detailed analysis at the block and chip levels at an optimized simulation time
- Manage and facilitate simulation with full parasitics
- Contain layout automation that can be used at appropriate points in the design
- Allow for several levels of passive modeling throughout the design process

These requirements must be met through a single environment that not only facilitates the job of the RFIC designer natively, but also integrates with other domains such as analog/mixed-signal (AMS) and digital. This must include both a chip- and block-level perspective at multiple abstraction levels, where the same design collateral can be passed back and forth facilitating verification and implementation from either environment point of view, independent of physical integration strategies.

## THE WIRELESS RFIC FLOW

Figure 2 depicts the wireless RFIC flow. The flow targets the RFIC designer and spans system design down to IC implementation, following the meet-in-the-middle approach described earlier.

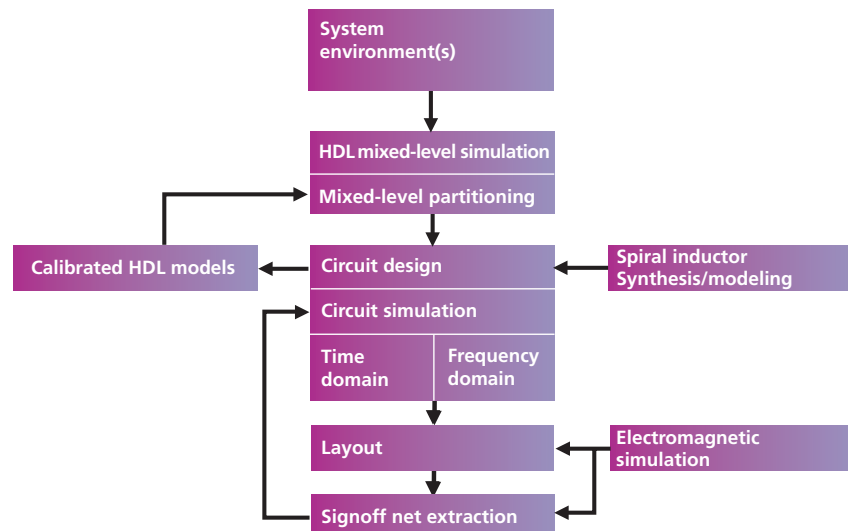


Figure 2: Wireless RFIC flow

### LEVERAGING SYSTEM-LEVEL CONTENT

The design collateral from the system design process is used as the first and highest abstraction level. System-level descriptions become an executable testbench for the top-level chip. Models of the surrounding system can be combined with a high-level model of the chip, producing an executable specification. System requirements serve as the first specification to drive the chip-level requirements, and ultimately turn into repeatable testbenches and regression simulations. Part of the leveraged system-level content is also the IP that determines the system-relevant figures of merit, like EVM, BER, and PER.

Mixed-level simulation allows a natural sharing of information between the system and block designers. To enable the required links from the system environment to the IC environment, it is essential that the underlying multi-mode simulation solution is language neutral (from system models in C/C++, SystemC®, and SystemVerilog to digital/mixed-signal/analog behavioral HDL languages to SPICE) and provides different engines and algorithms dedicated to the specific needs for a multi-domain circuit design.

### DESIGN PLANNING AND SIMULATION STRATEGY

Successful execution on a complex design is contingent on thorough upfront planning. No design comes together smoothly by accident. With a strong initial plan that specifies which top-level requirements, block-level requirements, and mixed-level strategies to use, a meet-in-the-middle approach can drive each block design to ensure full coverage of important design specifications and smoothly allow blocks to have different schedule constraints. Therefore, the development of a comprehensive simulation strategy, which in turn leads to a modeling plan, is key.

After realizing a high-level executable specification, the process continues by identifying particular areas of concern in the design. Plans are then developed for how each area of concern will be verified. The plans specify how the tests are performed and which blocks are at the transistor level during the test. It is important to resist the temptation to specify and write models that are more complicated than necessary. Start with simple models and only model additional effects as needed.

A formal planning process generally results in more efficient and more comprehensive verification, meaning that more flaws are caught early and there are consequently fewer design iterations. The simulation and test plans are applied initially to the high-level description of the system, where they can be debugged quickly. Once available, they can be applied during the mixed-level simulations of the blocks, reducing the chance that errors will be found late in the design cycle.

## MULTI-MODE SIMULATION ENVIRONMENT

The top-down process starts with HDL modeling for the entire RFIC added to the system-level testbench. This would include all RF blocks along with any analog content and/or digital blocks. The first step is to behaviorally model the full chip within a top-level testbench, which would verify some system test such as EVM or BER. This at first verifies the partitioning, block functionality, and ideal performance characteristics of the IC. This behavioral setup then serves as the basis to facilitate mixed-level simulations, where blocks can be inserted at the transistor level and verified in a top-level context. This full-chip and system setup can serve as the regression template to allow for continuous verification as blocks mature, allowing for a continuous evolution approach through the entire design. This is important as any problems that are found can be detected at the earliest moment where time still exists to fix the problem and blocks can be designed in parallel to individual schedules.

Looking through the full simulation environment, several views of the same circuit will exist. This is likely to consist of a behavioral view, a pre-layout transistor-level view, and several views of parasitic information. As blocks mature, it may be necessary to add more transistor-level information to test RF/analog and RF/digital interfaces. This will require the use of a mixed-signal simulator capable of handling analog, digital, and RF descriptions and mixed behavioral-level with transistor-level abstractions. Pick the appropriate views of each block or sub-block and manage the runtime vs. accuracy tradeoffs through simulation options such as sending the transistors to a FastSPICE simulator or keeping the transistors in a full SPICE mode. This configuration is highly dependent on the circuit and sensitivity of the interfaces. The ability to manage these configurations effectively is key, as these are required to be repeatable. This provides an effective mechanism to set up the continuous regressions that support the ACD Methodology.

## BLOCK CIRCUIT DESIGN

A preliminary circuit design then takes place, allowing for early circuit exploration and a first-cut look at performance specifications. This early exploration leads to a top-level floorplan, which for RFIC is sensitive to noise concerns and block-level interconnect. At this stage, it is possible to synthesize passive components such as spiral inductors to spec, and do an initial placement of them on the chip. This enables two key activities: creating early models for spiral inductors that can be used in simulation before the block-level layouts are complete, and allowing for an initial analysis of mutual inductance between the spirals. Component models of each inductor can be generated within this context for use in these simulations.

Simulation is performed using the designer-preferred method, either in the frequency or time domain. This depends on the circuit, type of simulation, or amount to be simulated, and is a judgment call by the designer. A single PDK and associated environment allows for a smooth determination and selection of the simulation algorithm desired. Results are displayed through an appropriate display for the simulation type selected. As circuits are completed at block level, they are verified within the top-level context with behavioral stimulus and descriptions for the surrounding chip.

## PHYSICAL IMPLEMENTATION

Layout automation (automated routing, connectivity-driven layout, design-rule-driven layout, placement) can be used judiciously. The advantage to layout automation is that it's tied to the schematic and DRC rules and allows for productivity gains. Analog-capable routers can help with differential pairs and shielding wires, and allow for manual constraints per line. This allows for a physical design process that can also become repeatable just like the front-end process. It may take

some time and overhead to setup the initial tools, but this is made up as iterations are made through the design process. Engineering change orders (ECOs) are more effectively performed if a repeatable layout process is in place. This is weighed against highly sensitive circuitry, which demands a manual approach.

## PARASITIC EXTRACTION

As layout is complete, electromagnetic simulation (EM) can be used to provide highly accurate models for passive components. For example, several spiral inductors may be selected as highly critical and a target for EM simulation; these can be swapped by replacing the models that were created early in the design process, and mixed and matched with the existing models. The designer then has full control over managing the spiral modeling process, again having the ability to tradeoff runtime vs. accuracy at their discretion.

Net-based parasitic extraction becomes a key element of the process as layouts emerge. RF design is highly sensitive to parasitic effects. As such, the ability to manage different levels of parasitic information becomes paramount, as the designer can describe which areas, lines, and blocks to have progressively more or less parasitic information associated with them. Less sensitive interconnects may require RC only, whereas more sensitive lines may require RLC. For lines with spirals attached, these can be extracted fully with RLC plus the associated inductor component, even with substrate effects added for those lines that are the most sensitive. Again, the lines that contain a “full” extraction can be mixed and matched with the component models for passive components that were created earlier.

In addition, as the top-level layout emerges, analysis—especially substrate noise—is used to ensure that noisy circuits (such as digital logic and perhaps PLLs) are not affecting the highly sensitive RF circuits. Designers can check for this, and as they flag areas of concern, they can either modify the floorplan accordingly or add guardbands around the noisy circuitry. However, it is often impractical to both simulate the entire design at transistor level and include all the parasitic information. One approach is to extract calibrated behavioral models using the extracted view of the design blocks. But this will not capture the effects of the parasitics on the interconnect between blocks. So hierarchical extraction capabilities to extract only parasitics of the interconnect between design blocks needs to be supported.

## CALIBRATED HDL MODELS

Finally, as blocks are completed, the initial behavioral models can be backannotated for key circuit performance parameters, which can provide more accurate HDL-level simulation. While this will not account for every effect, it can add more realistic performance information at little runtime cost, allowing for faster level verification and perhaps reducing the amount of full transistor-level verification required.

In this way, the verification of a block by mixed-level simulation becomes a three-step process. First, the proposed block functionality is verified by including an idealized model of the block in system-level simulations. Next, the functionality of the block as implemented is verified by replacing the idealized model with the netlist of the block. This also allows the effect of the block’s imperfections on system performance to be observed. Finally, the netlist of the block is replaced by an extracted model. By comparing the results achieved from simulations that involved the netlist and extracted models, the functionality and accuracy of the extracted model can be verified. From then on, mixed-level simulations of other blocks are made more representative by using the extracted model of the block just verified rather than the idealized model.

When performed properly, bottom-up verification achieves detailed verification of very large systems. Behavioral simulation runs quickly because the details of the implementation are discarded while the details of the behavior are saved. Because the details of the implementation are discarded, the detailed behavioral models generated in a bottom-up verification process are useful as blocks mature or for third-party IP evaluation and reuse.

Especially for wireless systems including RF front ends, bottom-up verification is mandatory when verifying the performance of large systems. As mentioned earlier, RF system simulations at the transistor level (running thousands of cycles of the modulated signal) is often impractical. The use of advanced envelope analysis techniques instead of traditional transient simulation would only provide a speed-up by a factor of 10-20x. And even bottom-up extraction using traditional passband models, where the RF carrier is still present, won't provide the required speed-up. Only the combination of bottom-up model extraction techniques with so-called complex baseband or low-pass equivalent models (where the carrier signal is suppressed) will lead to simulation times that enable package-error-rate analysis at the full-chip level.

Generating behavioral models that include the detailed behavior of even simple blocks can be difficult and requires a specialized skill not commonly found in the design team. Therefore, automated tools and methodologies generate detailed behavioral models with verified accuracy and an open API to modify the existing templates according to specific application and/or technology needs are required.

## SUMMARY

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The wireless RFIC flow is a key element of the Cadence RF Design Methodology Kit, spanning system-level design down to RFIC implementation. The versatility of the Kit's interaction with other solutions, such as the AMS flow, enables the right solution to be applied to the right design task.

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